JVC

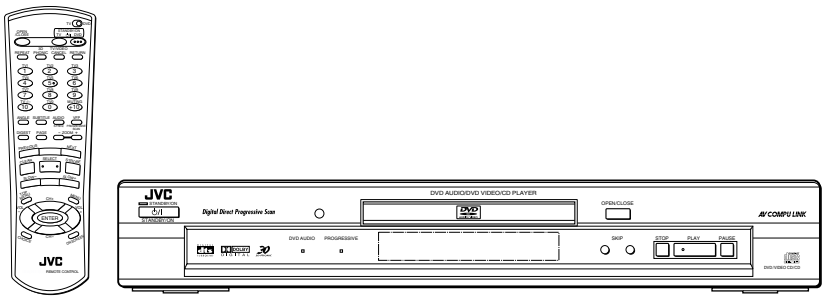
SERVICE MANUAL

DVD AUDIO/VIDEO PLAYER

XV-SA70BK / XV-SA75GD

Area Suffix (XV-SA70BK)
J ---------- U.S.A.
C ---------- Canada

Area Suffix (XV-SA75GD)
J ---------- U.S.A.



Each difference point

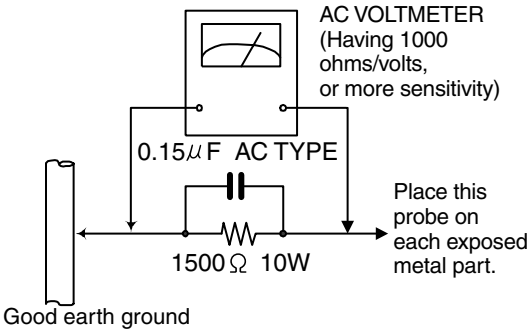
Model	Body color
XV-SA70BK	Black
XV-SA75GD	Gold

Contents

No.A0016
Jul. 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage current check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground. Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to each exposed metal part, particularly any exposed metal part having a return path to the chassis, and measure the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the J and C version)

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

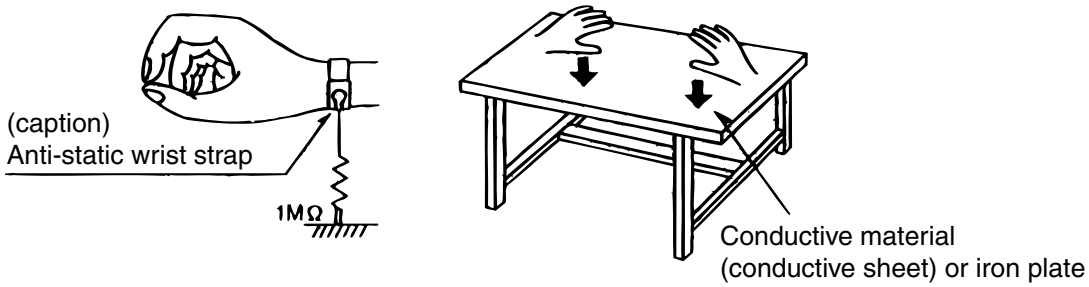
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

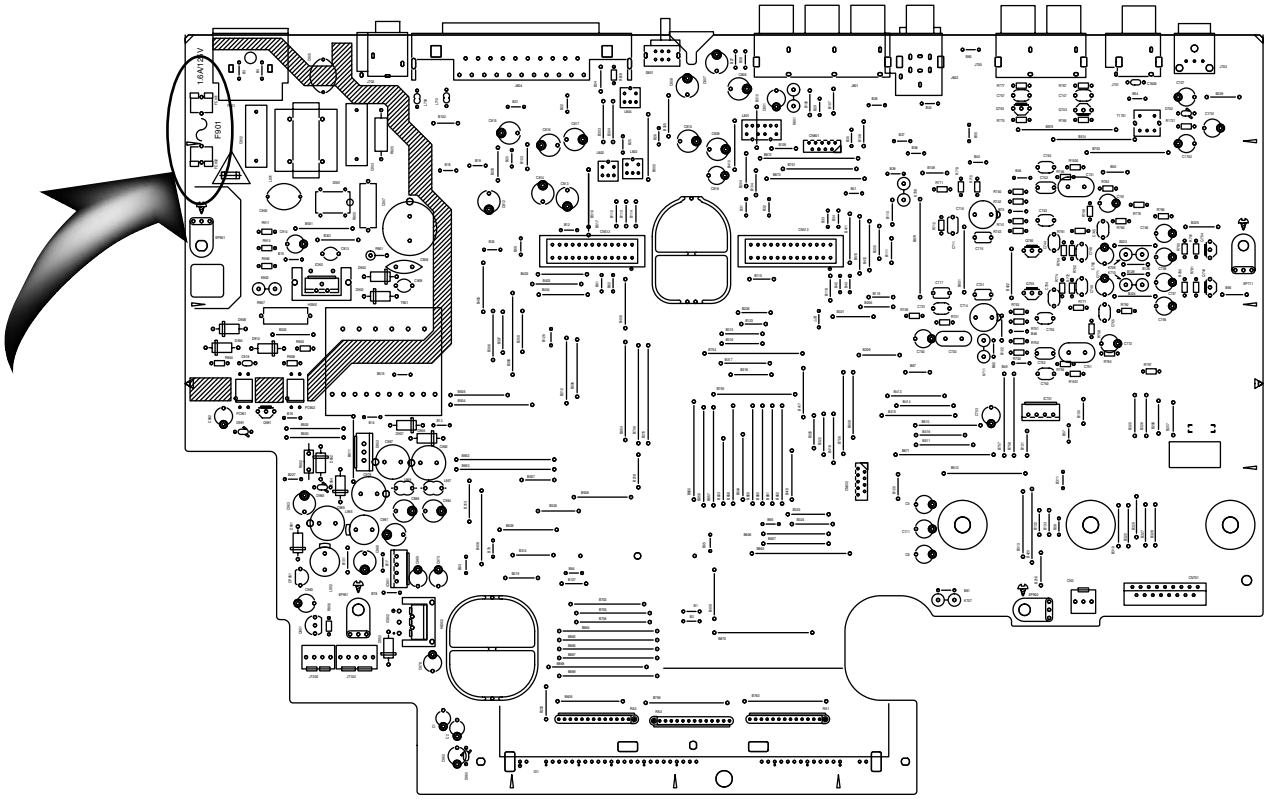
1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Importance Admistering point on the Safety



Full Fuse Replacement Marking	**Marquage Pour Le Remplacement Complet De Fusible**
Graphic symbol mark (This symbol means fast blow type fuse.) should be read as follows ;	Le symbole graphique (Ce symbole signifie fusible de type á fusion rapide.) doit être interprété comme suit ;
FUSE CAUTION	**PRECAUTIONS SUR LES FUSIBLES**
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSES ; **F901 : 1.6 A / 125 V**	**POUR UNE PROTECTION CONTINUE CONTRE DES RISQUES D'INCENDIE, REMPLACER SEULEMENT PAR UN FUSIBLE DU MEME TYPE ;** **F901 : 1.6 A / 125 V**

Precautions for Service

Handling of Traverse Unit and Laser Pickup

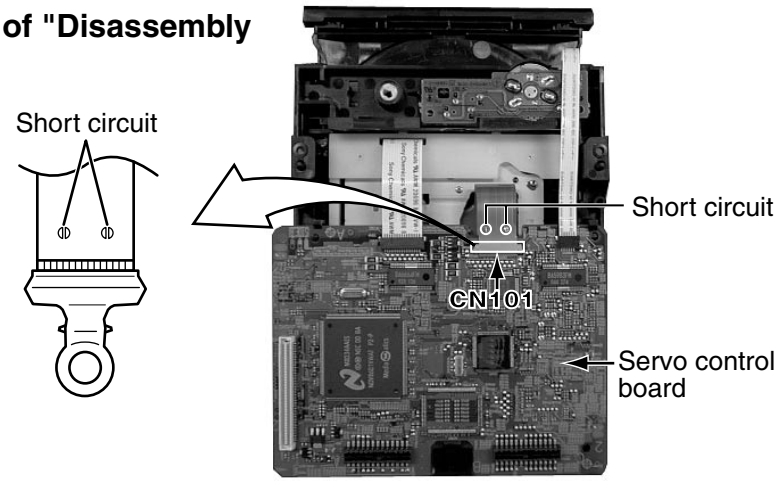
1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. After removing the flexible wire from the connector (CN101), short-circuit the flexible wire by the metal clip.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.
   After completing the repair, remove the solder to open the circuit.

Please refer to "Fig.5" of "Disassembly method" for details.



Disassembly method

<Main body>

■ Removing the top cover (see Fig.1)

1. Remove the two screws **A** attaching the top cover on both sides of the body.
2. Remove the three screws **B** attaching the top cover on the back of body.
3. Remove the top cover from the body by lifting the rear panel of top cover.

ATTENTION : Do not break the front panel tab fitted to the top cover.

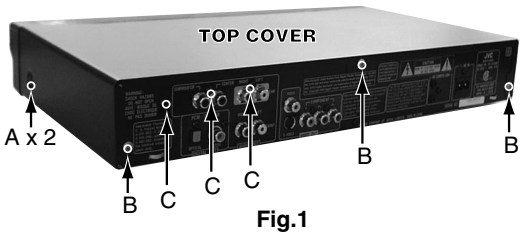


Fig.1

■ Removing the surround audio board (see Fig.1,2)

*Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from connector CN711 on the surround audio board.
2. Remove the three screws **C** attaching the surround audio board on the rear panel.
3. The surround audio board is removed while picking up the point of the fastener in two places.

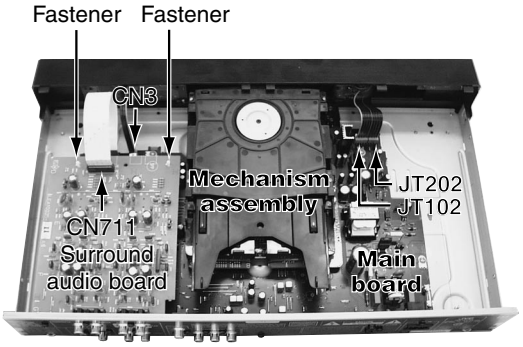


Fig.2

■ Removing the mechanism assembly (see Fig.3,4)

*Prior to performing the following procedure, remove the top cover.
*There is no need to remove the front panel assembly.

1. Remove the three screws **D** attaching the mechanism assembly on the bottom chassis.
2. The servo control board is removed from the connector CN512 and CN513 connected with the main board respectively.
3. Remove the mechanism assembly by lifting the rear part of the mechanism assembly.

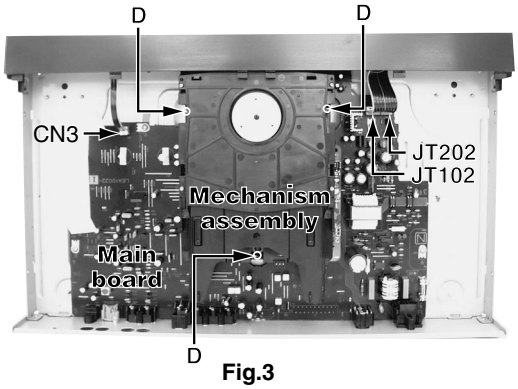


Fig.3

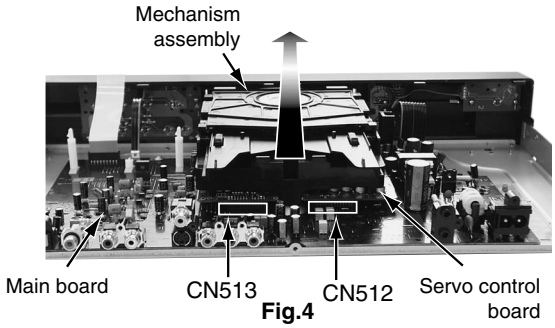


Fig.4

■ Removing the servo control board (see Fig.5)

*Prior to performing the following procedure, remove the top cover and mechanism assembly.

1. Disconnect the card wire from connector CN201 and CN202 on the servo control board respectively.
2. Disconnect the flexible wire from connector CN101 on the servo control board from pick-up.

ATTENTION
At this time, please extract the wire after short-circuited of two places on the wire in part **a** with solder.
Please remove the solder two places of part **a** after connecting the wire with CN101 when reassembling.

3. Two places in hook **b** are removed, the servo control board is lifted, and it is removed.

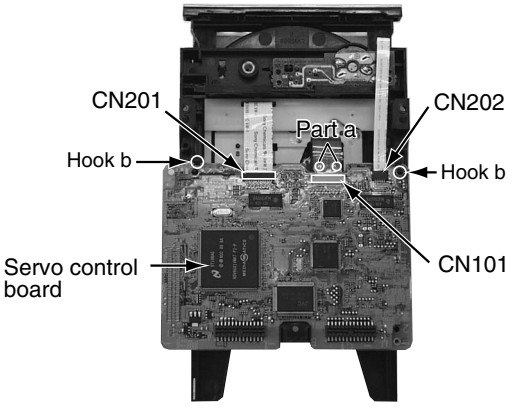


Fig.5

■ Removing the rear panel (see Fig.6)

*Prior to performing the following procedure, remove the top cover.

1.Remove the twelve screws **E** attaching the rear panel on the back of body.

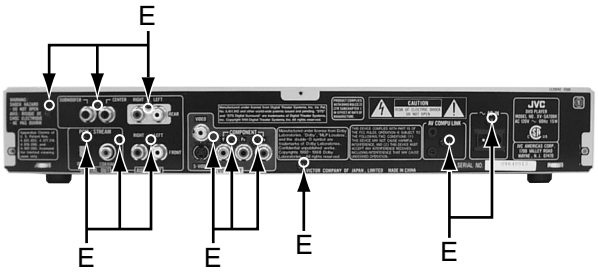


Fig.6

■ Removing the front panel assembly (see Fig.7,8)

* Prior to performing the following procedure, remove the top cover.
* There is no need to remove the mechanism assembly.

1.Remove the one screw **F** attaching the front panel assembly on the bottom chassis.

2.Remove the four screws **G** attaching the foot on the bottom chassis.

3.Disconnect the wire from CN3, JT102 and JT202 on the main board respectively.

4.Hook **c** and **d** are removed respectively, and the front panel assembly is removed.

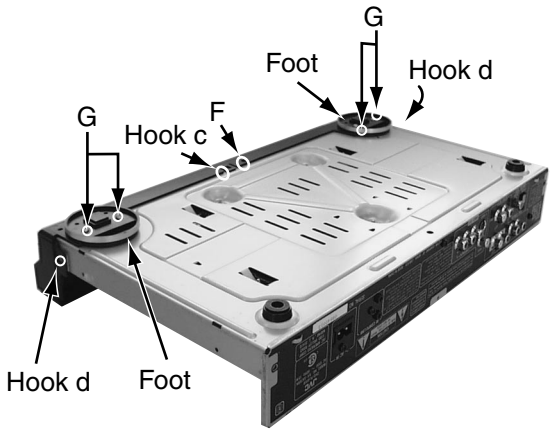


Fig.7

■ Removing the main board (see Fig.9)

* Prior to performing the following procedure, remove the top cover, surround audio board, mechanism assembly and rear panel.

1.Disconnect the wire from CN3, JT102 and JT202 and on the main board respectively.

2.Remove the four screws **H** attaching the main board on the bottom chassis.

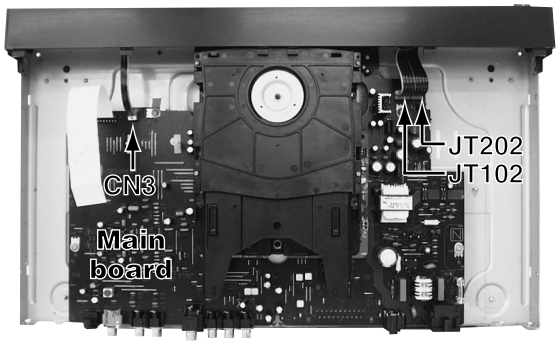


Fig.8

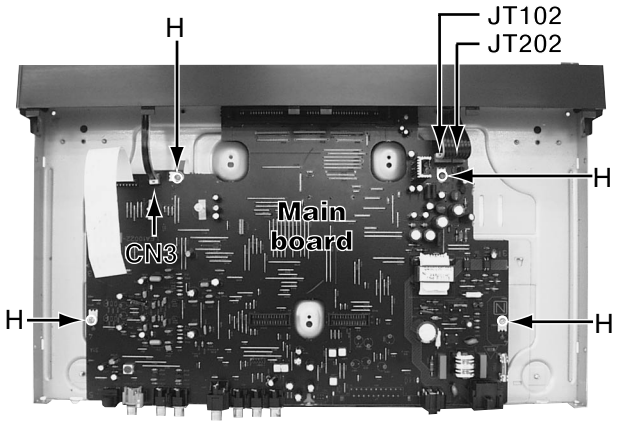


Fig.9

<Loading assembly section>

■ Removing the clamper assembly (See Fig.1)

1. Remove the four screws **A** attaching the clamper assembly.

2. Move the clamper in the direction of the arrow to release the two joints **a** on both sides.

ATTENTION: When reattaching, fit the clamper to the two joints **a**.

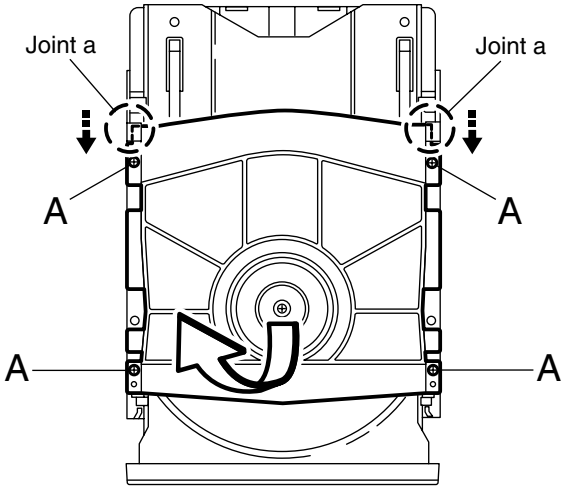


Fig.1

■ Removing the tray (See Fig.2 and 3)

・ Prior to performing the following procedure, remove the clamper assembly.

1. Push **b** of the slide cam into the slot on the left side of the loading base until it stops.

2. Draw out the tray toward the front.

ATTENTION: Before reattaching the tray, slide the part **c** of the slide cam to the right as shown in Fig.3.

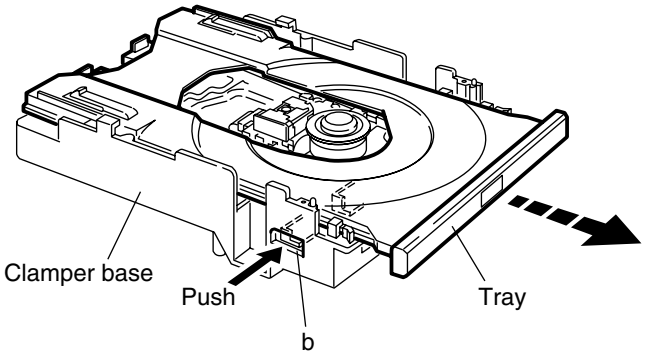


Fig.2

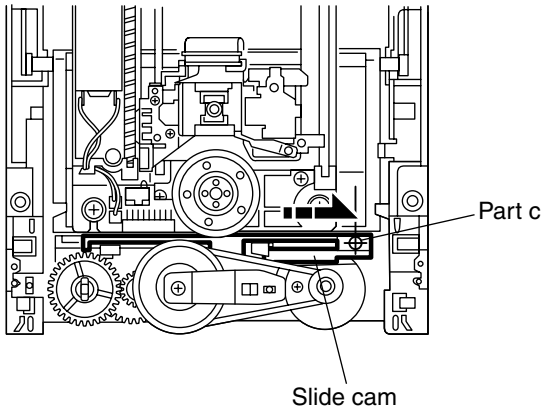


Fig.3

■Removing the traverse mechanism assembly (See Fig.4 and 5)

・ Prior to performing the following procedure, remove the clamper assembly and the tray.

1. Remove the four screws **B** attaching the traverse mechanism assembly.

ATTENTION: Before reattaching the traverse mechanism assembly, pass the card wire extending from the spindle motor board through the notch **d** of the elevator.

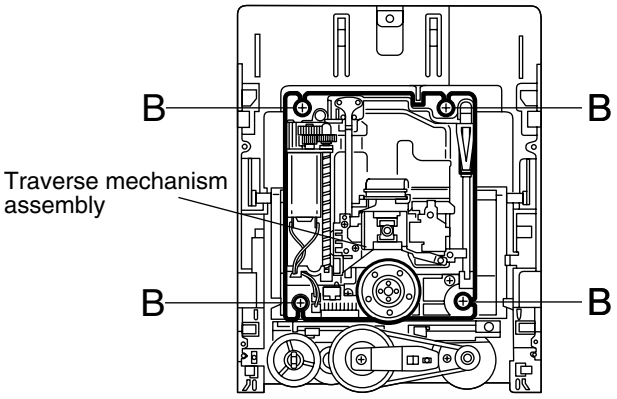


Fig.4

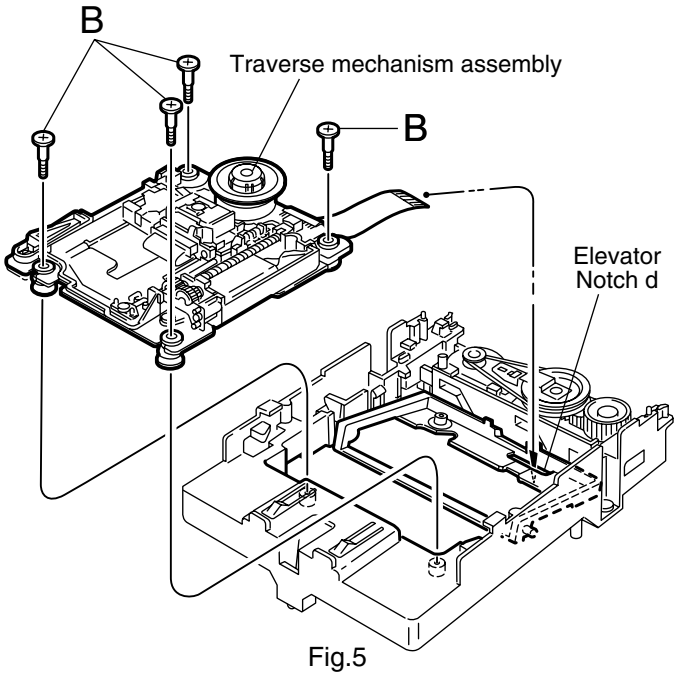


Fig.5

■Removing the elevator (See Fig.6 and 7)

・ Prior to performing the following procedure, remove the clamper assembly, the tray and the traverse mechanism assembly.

1. Extend each bar **e** inside of the loading base outward and detach the elevator shaft.

ATTENTION: When reattaching, first fit the two shafts on the front of the elevator to the slots **f** of the slide cam.

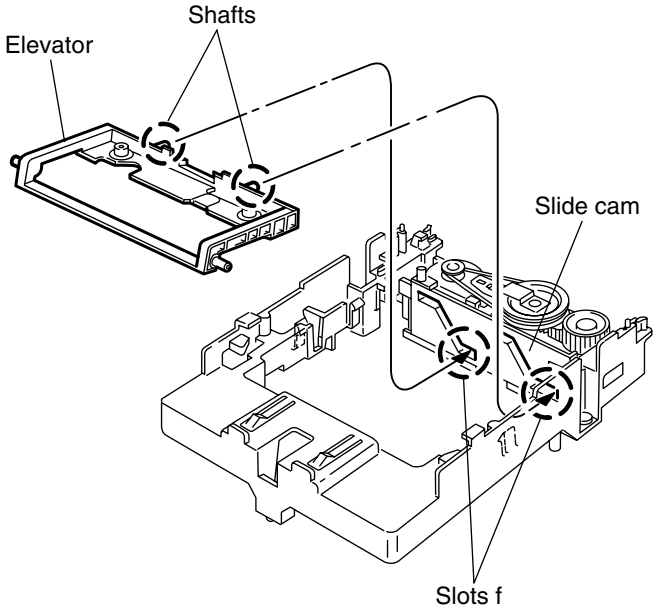


Fig.7

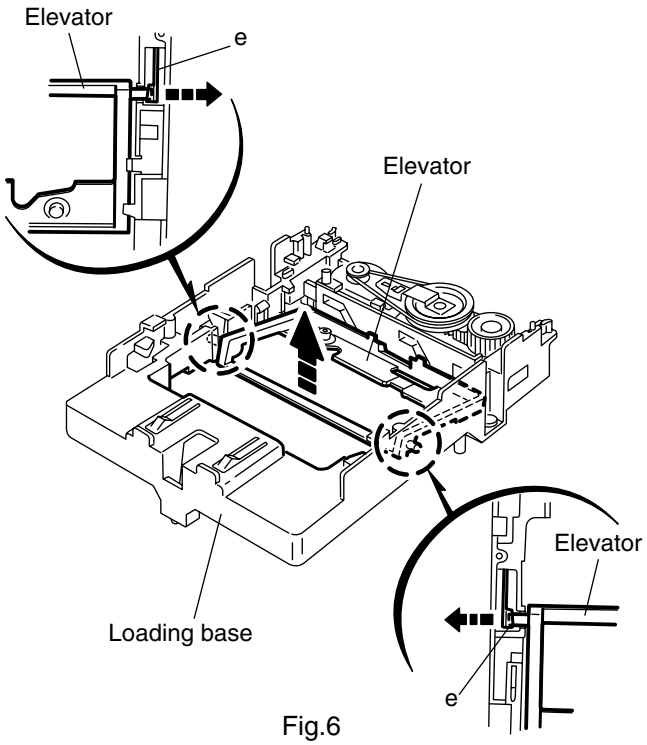


Fig.6

■ Removing the motor assembly (See Fig.8 and 9)

- Prior to performing the following procedure, remove the clamper assembly, the tray, the traverse mechanism assembly and the elevator.

1. Remove the belt from the pulley.
2. Remove the screw **C** attaching the motor assembly.
3. Turn over the body and remove the screw **D** attaching the motor assembly.
4. Release the two tabs **g** retaining the motor board.

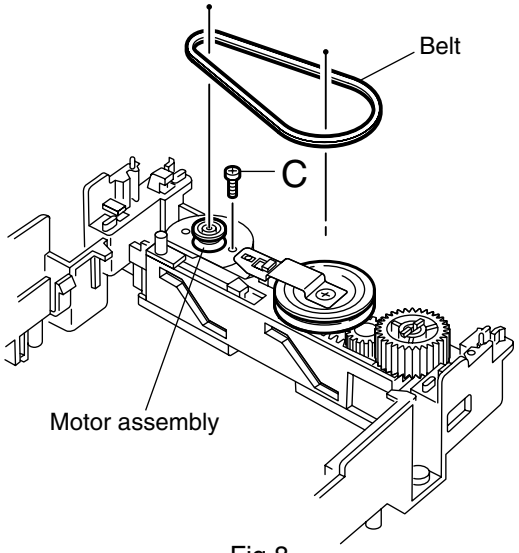


Fig.8

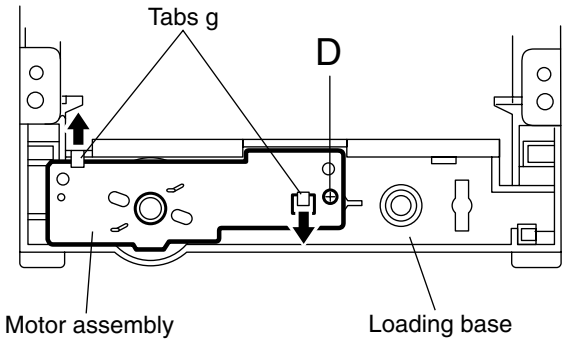


Fig.9

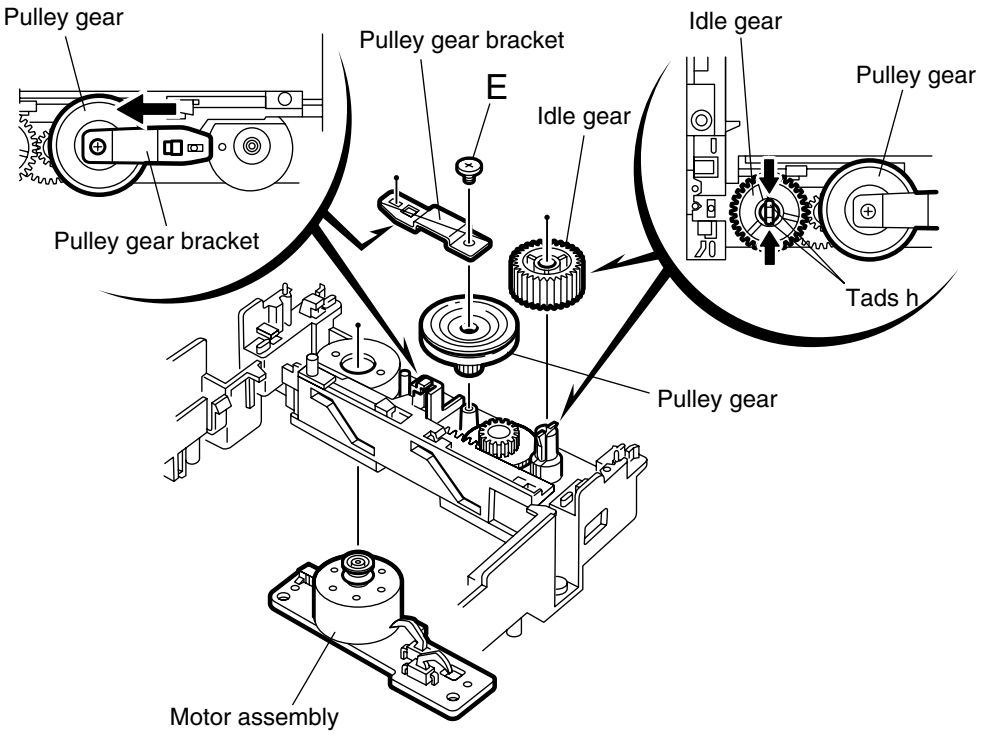


Fig.10

■Removing the Idle gear / pulley gear / middle gear / slide cam (See Fig.10 to 12)

・ Prior to performing the following procedure, remove the clamper assembly, the tray, the traverse mechanism assembly, the elevator and the motor assembly.

1. Press the two tabs **h** inward and pull out the idle gear.

2. Remove the screw **E** attaching the pulley gear bracket. Slide the pulley gear bracket in the direction of the arrow and pull out the pulley gear.

3. Slide the slide cam in the direction of the arrow to release the two joints **i** and remove upward.

4. Remove the middle gear.

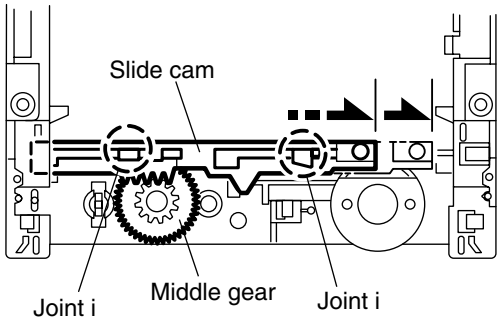


Fig.11

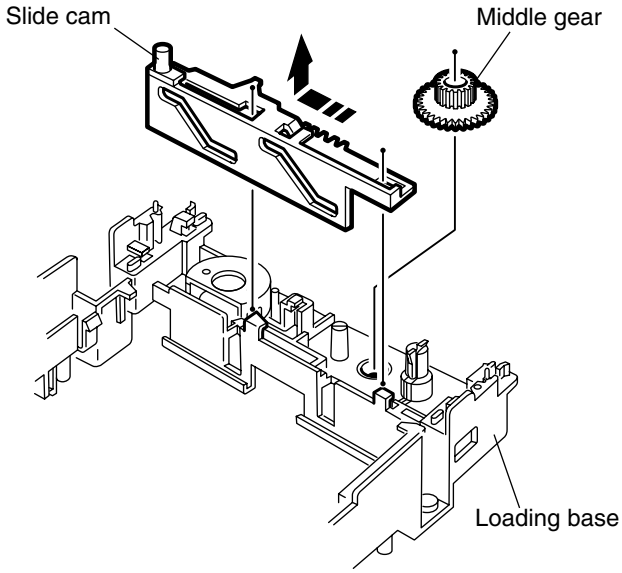


Fig.12

<Traverse mechanism assembly section>

■ Removing the feed motor assembly (See Fig.13)

1. Unsolder the two soldering **j** on the spindle motor board.

2. Remove the two screws **F** attaching the feed motor assembly.

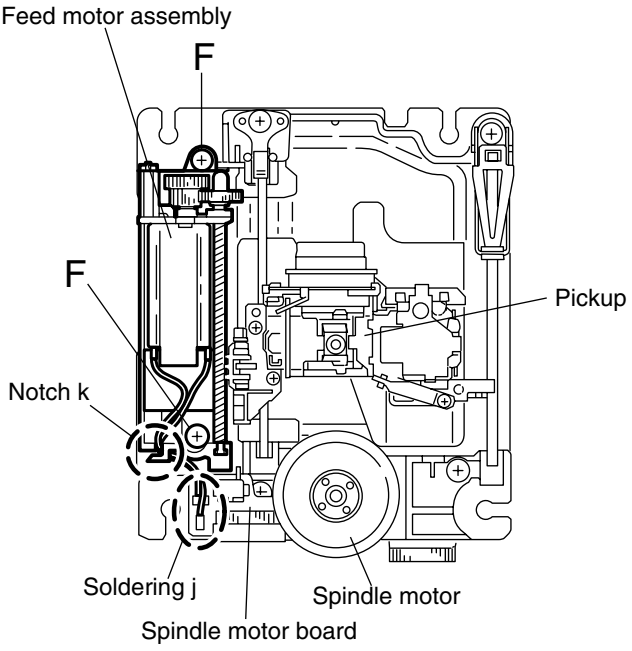


Fig.13

■ Removing the feed motor (See Fig.13 to 15)

・ Prior to performing the following procedure, remove the feed motor assembly.

1. Remove the screw **G** attaching the thrust spring.

ATTENTION: When reattaching the thrust spring, make sure that the thrust spring presses the feed gear (M) and the feed gear (E) reasonably.

2. Remove the feed gear (M).

3. Pull out the feed gear (E) and the lead screw.

4. Remove the two screws **H** attaching the feed motor.

ATTENTION: When reattaching, pass the two cables extending from the feed motor through the notch **k** of the feed holder as shown in Fig.13.

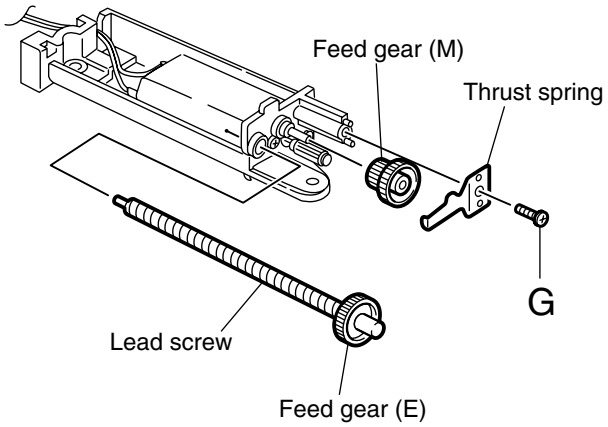


Fig.14

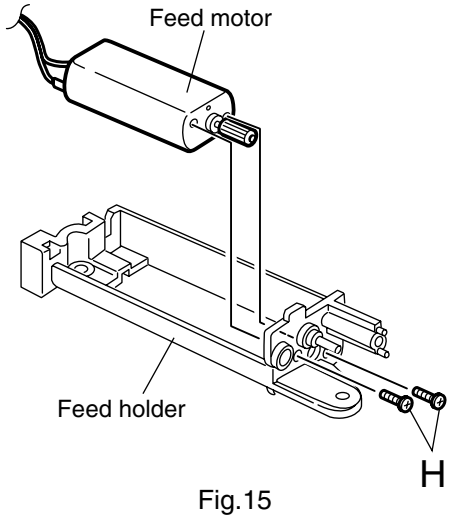


Fig.15

■ Removing the pickup (See Fig.16 and 17)

1. Remove the screw **I** attaching the T spring (S) and the shaft holder. Remove also the plate.

ATTENTION: When reattaching, make sure that the T spring (S) presses the shaft.

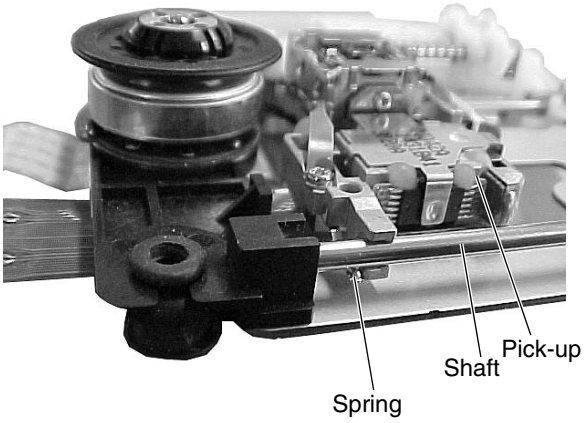
2. Pull out the part **l** of the shaft upward. Move the part **m** in the direction of the arrow and detach from the spindle base.

3. Disengage the joint **n** of the pickup and the shaft in the direction of the arrow.

4. Pull out the shaft from the pickup.

5. Remove the two screws **J** attaching the actuator.

6. Disengage the joint of the actuator and the lead spring. Pull out the lead spring.



The spring must be under the shaft when you install pick-up.

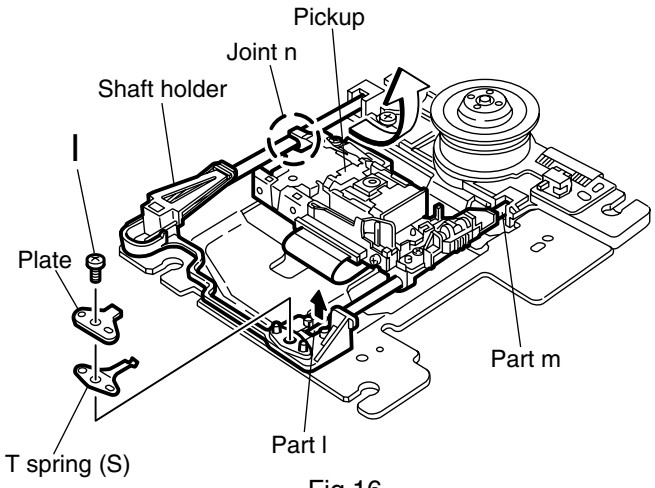


Fig.16

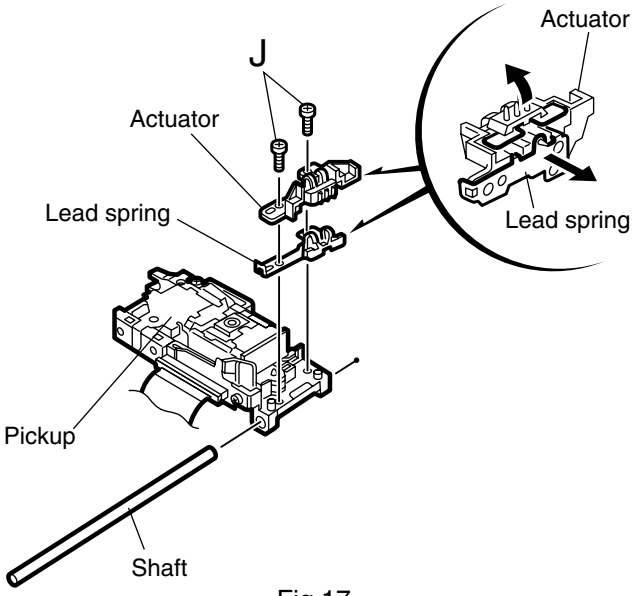


Fig.17

■ Removing the shaft holder / shaft (See Fig.18)

1. Remove the screw **K** attaching the shaft holder.

2. Remove the shaft.

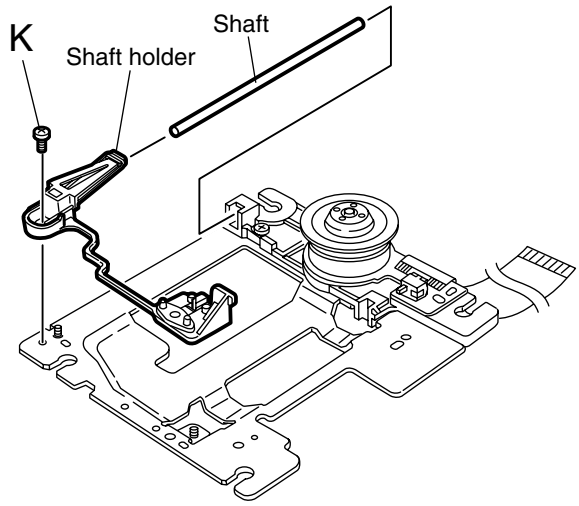


Fig.18

■ Removing the spindle motor assembly (See Fig.19 to 21)

1. Remove the three screws **L** attaching the spindle motor on the bottom of the mechanism base.

ATTENTION: When reattaching, pass the card wire extending from the spindle motor board through the notch of the spindle base.

2. Remove the three screws **M** attaching the spindle base.

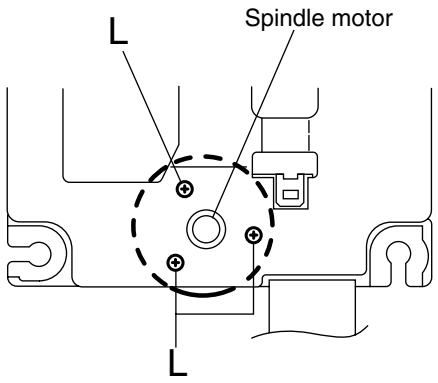


Fig.19

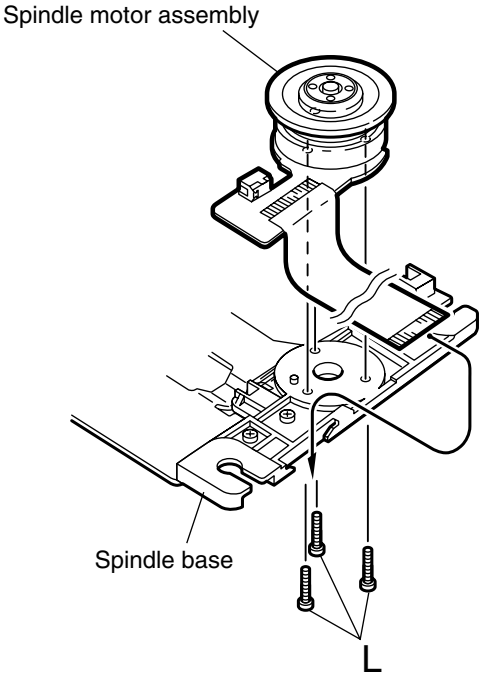


Fig.20

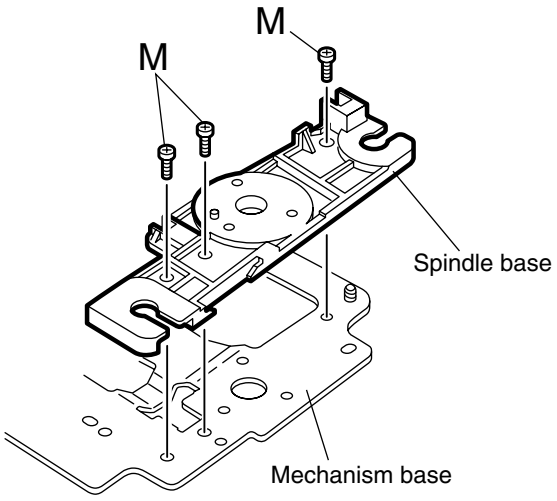


Fig.21

Adjustment method

(1) Test mode setting method

1)Take out the disc and close the tray.
2)Unplug the power plug.
3)Insert power plug into outlet while pressing both "PLAY" button and "STOP" button of the main body.
4)The player displays "TEST ＊＊ " on the FL display. " ＊＊" means the player version.
5)When the power supply is turned off, test mode is released.

The mode changes as follows whenever the "CHOICE" button of remote control is pushed in test mode.

TEST_＊＊_＊	Becomes test mode
＊＊＊＊＊＊＊＊＊＊＊＊	Device key index
＊＊_＊＊_＊＊_＊＊	Version of microcomputer
CHECK	Check mode
FL display becomes all lighting	Confirmation of FL display
＊＊＊＊_＊＊＊＊	Not use mode

(2) Initialization method

Please initialize according to the following procedures when microprocessor or pick-up is exchanged and when the up-grade is done.

1)Makes to test mode.
2)After "FORWARD SKIP" button (▶▶|) of the main body is pushed, "PAUSE" button is pushed.
3)DVD AUDIO indicator lights when about ten seconds pass. Then, it is initialization completion.

(3) Method of displaying device key index

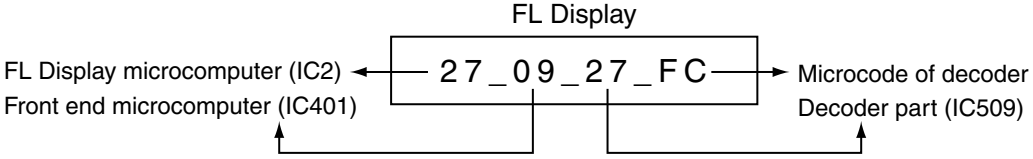
1)Makes to test mode and initializes.
2)When "CHOICE" button of remote control is pushed once, the device key index is displayed on the FL display as follows.

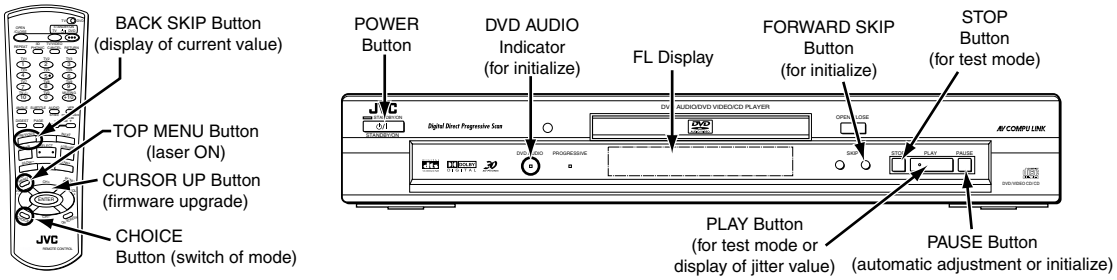
FL Display

＊＊＊＊＊＊＊＊＊＊＊ ＊ is a figure or an alphabet.

(4) Method of displaying version of microcomputer

1)Makes to test mode and initializes
2)When "CHOICE" button of remote control is pushed twice, the figure is displayed on the FL display as follows.





(5) Display of current value of laser

1)Makes to test mode and initializes
2)When "CHOICE" button of remote controller is pushed three times, It is displayed on the FL display, "CHECK".
3)The display of FL display changes from "CHECK" into "LD_ON" if the "TOP MENU" button of remote controller is pushed.
4)The laser is turned on if the "BACK SKIP" button (⏮) of remote controller is pushed in the state, and the current value of the laser is displayed on the FL display.

FL Display

LD_0034

As for the current value of the laser, the figure displayed on the FL display becomes a current value as it is by "mA" unit. becomes 34mA if displayed as 34.

5)The laser changes from CD into DVD if 3) and 4) of the above-mentioned procedures are done after the tray is opened and closed pushing the "OPEN/CLOSE" button of the main body. (The laser changes whenever this is done.)

If the laser current value is 64mA or less, it is roughly good. There is a possibility to which pick-up is deteriorated, and exchange pick-up, please when there are 65mA or more laser current value.

(6) Display of jitter value

1)Makes to test mode and initializes
2)When "CHOICE" button of remote controller is pushed three times, It is displayed on the FL display, "CHECK".
3)The automatic adjustment starts when test disk (VT-501) is inserted, and "PAUSE" button of the main body is pushed.
4)When the display of the FL display changes into "CHECK OK", the "PLAY" button of the main body is pushed.
5)The jitter value is displayed on the FL display as follows.

FL Display

JIT_3978

The jitter value is displayed by the hexadecimal number and refer to the conversion table of following, please.

If the indication value is 11% or less, it can be judged by this simple checking method that the signal read precision of the set is satisfactory.
Please do "Flap adjustment of the pick-up guide shaft" when you replace the pick-up and the spindle motor when there are 11% or more jitter value.

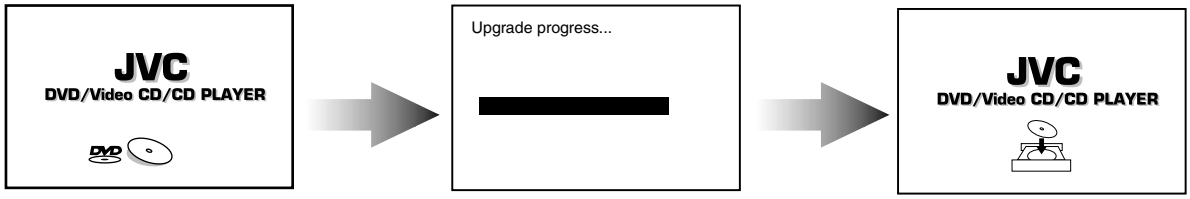
■ Jitter value

FL display	Conversion value(%)	FL display	Conversion value(%)	FL display	Conversion value(%)	FL display	Conversion value(%)
3818	4.7	3998	7.6	3B18	10.5	3C98	13.3
3828	4.8	39A8	7.7	3B28	10.6	3CA8	13.5
3838	4.9	39B8	7.8	3B38	10.7	3CB8	13.6
3848	5.1	39C8	7.9	3B48	10.8	3CC8	13.7
3858	5.2	39D8	8.1	3B58	10.9	3CD8	13.8
3868	5.3	39E8	8.2	3B68	11.1	3CE8	13.9
3878	5.4	39F8	8.3	3B78	11.2	3CF8	14.1
3888	5.5	3A18	8.5	3B88	11.3	3D18	14.3
3898	5.7	3A28	8.7	3B98	11.4	3D28	14.4
38A8	5.8	3A38	8.8	3BA8	11.5	3D38	14.5
38b8	5.9	3A48	8.9	3BB8	11.7	3D48	14.7
38c8	6.0	3A58	9.0	3BC8	11.8	3D58	14.8
38d8	6.1	3A68	9.1	3BD8	11.9	3D68	14.9
38E8	6.3	3A78	9.3	3BE8	12.0	3D78	15.0
38F8	6.4	3A88	9.4	3BF8	12.1	3D88	15.1
3918	6.6	3A98	9.5	3C18	12.4	3D98	15.3
3928	6.7	3AA8	9.6	3C28	12.5	3DA8	15.4
3938	6.9	3AB8	9.7	3C38	12.7	3DB8	15.5
3948	7.0	3AC8	9.9	3C48	12.7	3DC8	15.6
3958	7.1	3AD8	10.0	3C58	12.9	3DD8	15.7
3968	7.2	3AE8	10.1	3C68	13.0	3DE8	15.9
3978	7.3	3AF8	10.2	3C78	13.1	3DF8	16.0
3988	7.5			3C88	13.2		

(7) Upgrading of firmware

Please do the up-grade of the firmware after exchanging IC509,IC512,IC513.

1)The power supply is turned on pushing the "POWER" button.
2)The up-grade disk is inserted.
3)When FL display of the main body changes from "READING" into "UPGRADE", cursor UP button (▲) of remote controller is pushed.
4)The up-grade starts if the entire screen becomes blue and it is displayed, "Upgrade progress".
5)The tray opens automatically, the up-grade disk is removed.
6)The up-grade ends if the tray closes automatically, and the screen returns to the normal screen.
7)Please confirm the version of the microcomputer after makes to test mode and initializes.



After inserting the up-grade disk　　Upgrading (blue screen)　　When up-grade is completed

The disk for the up-grade is usually one piece. The disk becomes two pieces according to the version. In that case, please note the undermentioned content.

* The up-grade is done by using the STEP1 disk according to "1)" and "4)" of the above-mentioned procedure.
* The tray opens automatically after a few seconds and exchange for the disk of STEP2, please.
* The tray closes automatically. There is only about five second time that the tray opens this time, and replace the disk quickly between those, please.

ATTENTION

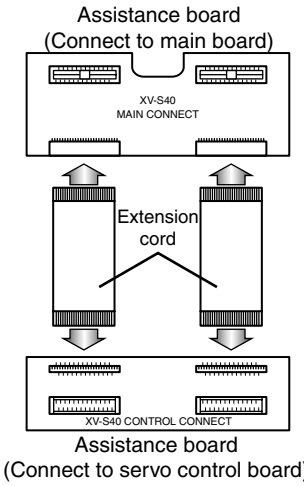
- When the tray shuts with the STEP1 disk left for the tray
  The up-grade starts again and exchange for the STEP2 disk, please when the tray opens automatically.
- When the tray closes with there no disk in the tray
  The tray opens automatically and turn off the power supply once, please pushing the "POWER" button in the state. When the STANDBY indicator lights, the STEP2 disk is putting in the tray and "POWER" button is pushed.

* After the up-grade ends, the STEP2 disk is removed because the tray opens automatically.
* Afterwards, it is the same as 6),7) of the above-mentioned procedures.

■ Flap adjustment of the pick-up guide shaft

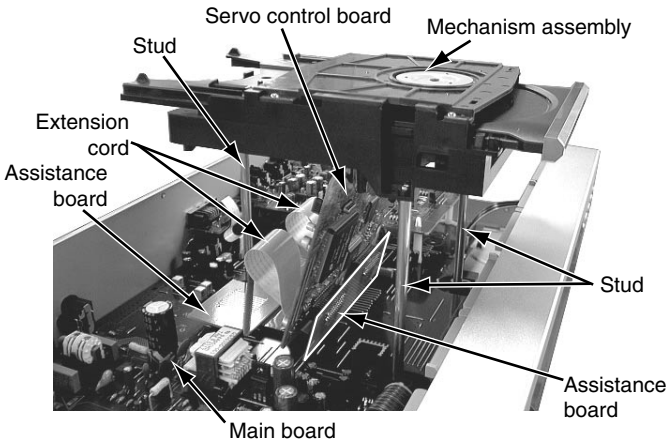
<Tool list for adjustment>

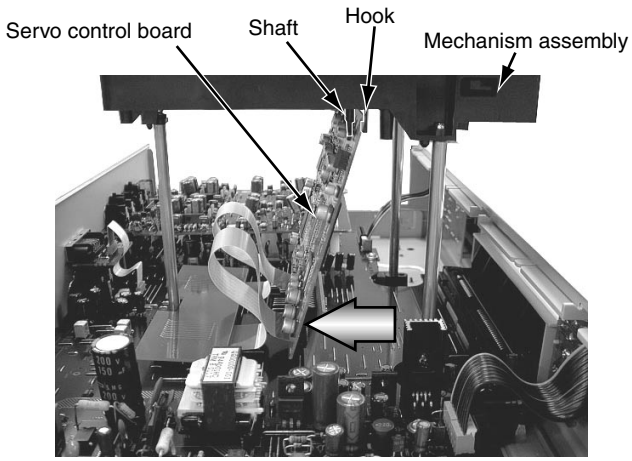
Stud (four pieces set)
Parts No. : JIGXVS40
Extension cord set (two cord and two board)
Parts No. : EXTXVS40CB
Hex wrench for adjustment
Off-the-shelf (1.3mm)
Test disc
VT-501 or VT-502



<Adjustment preparation>

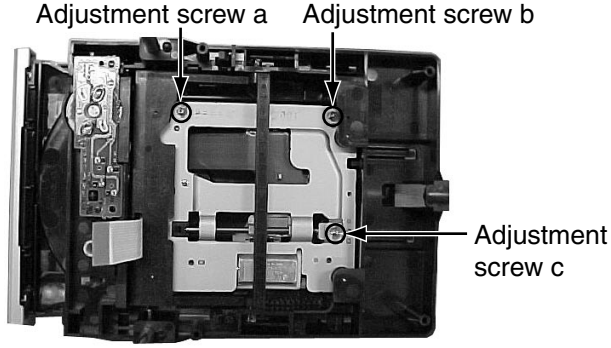
1. The mechanism assembly is made in the state from the main body from which is detached referring to the disassembly method.
2. Three studs are installed in the mechanism assembly respectively.
3. The servo control board is removed from the mechanism assembly, and puts into the state set up as shown in figure. (Each wire connected by the servo control board this time leaves the connection maintained.) Between shaft and hook of mechanism assembly of figure Board is put And, the board is inclined in the direction of the arrow on figure as much as possible.
4. The extension cord is inserted in the connector of the assistance board respectively. The main board is connected with the servo control board as shown in figure.





<Adjustment>

1. Puts into the state to display the jitter value on the FL display referring to "Display of the jitter value".
2. The adjustment screw under the traverse mechanism is turned with hex wrench, and matches so that the jitter value displayed on the FL display may become minimum value.

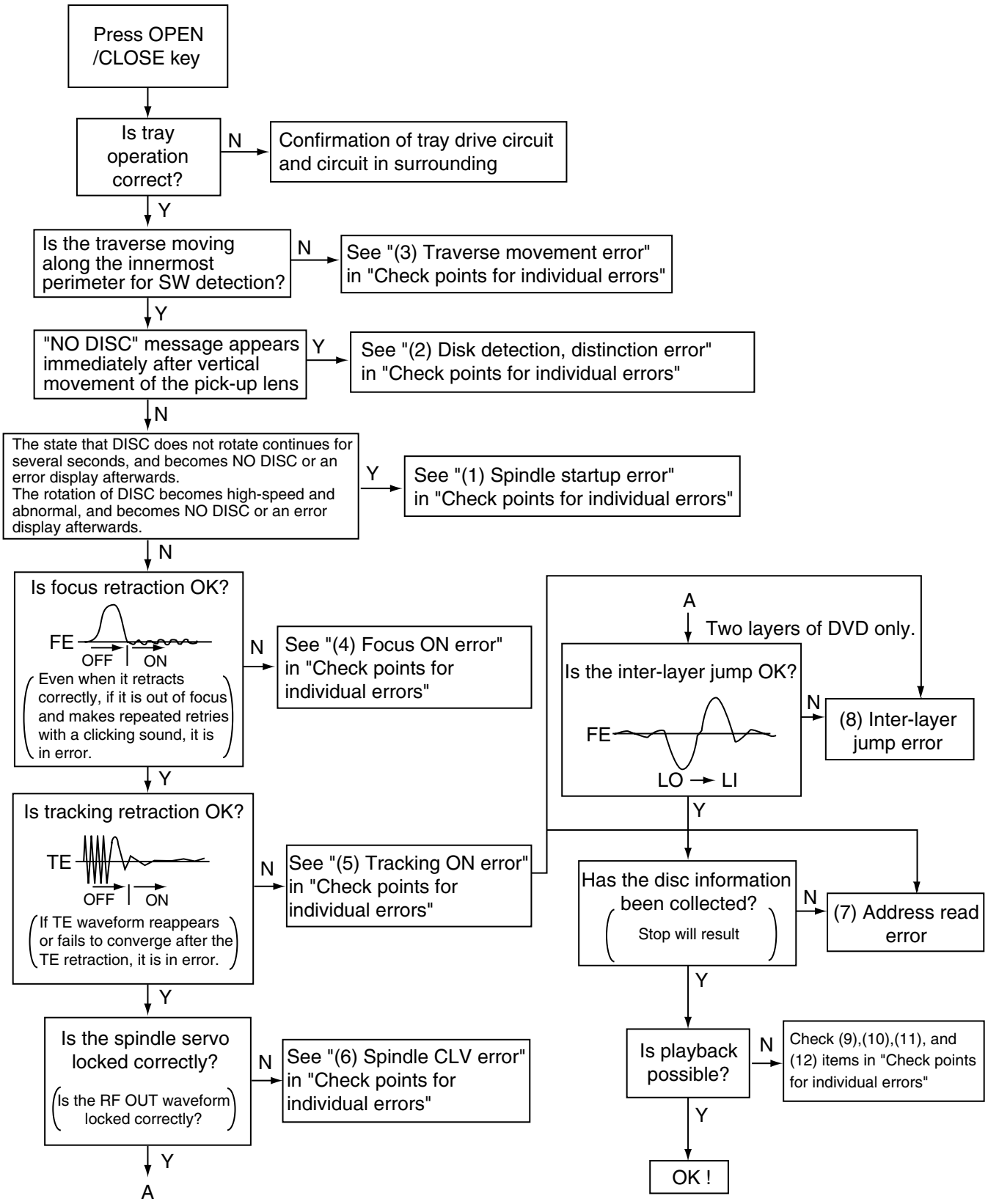


<POINT>

1. turns in the forward or the opposite direction, and makes to the position where the jitter value is good the half rotation of adjustment screw a and b(180 degrees) respectively.
2. Afterwards, adjustment screw b and c are turned in the same way, and makes to the best position.

Troubleshooting

Servo volume



Check points for each error

(1) Spindle start error

1.Defective spindle motor

*Are there several ohms resistance between each pin of CN201 "5-6","6-7","5-7"?
(The power supply is turned off and measured.)

*Is the sign wave of about 100mVp-p in the voltage had from each terminal?
[CN201"9"(H1-),"10"(H1+),"11"(H2-),"12"(H2+),"13"(H3-),"14"(H3+)]

2.Defective spindle motor driver (IC251)

*Has motor drive voltage of a sine wave or a rectangular wave gone out to each terminal(SM1~3)
of CN201"5,6,7" and IC251"2,4,7"?

*Is FG pulse output from the terminal of IC251"24"(FG) according to the rotation of the motor?

*Is it "L(about 0.9V)" while terminal of IC251"15"(VH) is rotating the motor?

3.Has the control signal come from servo IC or the microcomputer?

*Is it "L" while the terminal of IC251"18"(SBRK) is operating?
Is it "H" while the terminal of IC251"23"(/SPMUTE) is operating?

*Is the control signal input to the terminal of IC251"22"(EC)?
(changes from VHALF voltage while the motor is working.)

*Is the VHALF voltage input to the terminal of IC251"21"(ECR)?

4.Is the FG signal input to the servo IC?

*Is FG pulse input to the terminal of IC201"53"(FG) according to the rotation of the motor?

(2) Disc Detection, Distinction error (no disc, no RFENV)

* Laser is defective.
* Front End Processor is defective (IC101).
* APC circuit is defective. --- Q101,Q102.
* Pattern is defective. --- Lines for CN101 - All patterns which relate to pick-up and patterns between IC101
* Servo IC is defective (IC201).
* IC101 --- For signal from IC101 to IC201, is signal output from IC101 "20" (ASOUT) and
IC101 "41"(RFENV) and IC101 "22" (FEOUT)?

(3) Traverse movement NG

1.Defective traverse driver
*Has the voltage come between terminal of CN101 "1" and "2" ?

2.Defective BTL driver (IC271)
*Has the motor drive voltage gone out to IC271"17" or "18"?

3.Has the control signal come from servo IC or the microcomputer?
*Is it "H" while the terminal of IC271"9"(STBY1) ?
*TRSDRV Is the signal input? (IC201 "51")

4.TRVSW is the signal input from microcomputer? (IC401 "50")

(4) Focus ON NG

* Is FE output ? --- Pattern, IC101
* Is FODRV signal sent ? (R279) --- Pattern, IC201 "5"
* Is driving voltage sent ?
  IC271 "13", "14" --- If NG, pattern, driver, mechanical unit .
* Mechanical unit is defective.

(5) Tracking ON NG

* When the tracking loop cannot be drawn in, TE shape of waves does not settle.
* Mechanical unit is defective.
  Because the self adjustment cannot be normally adjusted, the thing which cannot be normally drawn in is thought.
* Periphery of driver (IC271)
  Constant or IC it self is defective.
* Servo IC (IC201)
  When improperly adjusted due to defective IC.

(6) Spindle CLV NG

* IC101 -- "35"(RF OUT), "30"(ARF-), "31(ARF+).
* Does not the input or the output of driver's spindle signal do the grip?
* Has the tracking been turned on?
* Spindle motor and driver is defective.
* Additionally, "IC101 and IC201" and "Mechanism is defective(jitter)", etc. are thought.

(7) Address read NG

* Besides, the undermentioned cause is thought though specific of the cause is difficult because various factors are thought.
  Mechanism is defective. (jitter)
  IC201, IC301, IC401.
  The disc is dirty or the wound has adhered.

(8) Between layers jump NG (double-layer disc only)

Mechanism defective
Defect of driver's IC(IC271)
Defect of servo control IC(IC201)

(9) Neither picture nor sound is output

1.It is not possible to search
*Has the tracking been turned on?
*To "(5) Tracking ON NG" in "Check points for each error" when the tracking is not normal.
*Is the feed operation normal?
To "(3) traverse movement NG" in "Check points for each error" when it is not normal.
Are not there caught of the feeding mechanism etc?

(10) Picture is distorted or abnormal sound occurs at intervals of several seconds.

Is the feed operation normal?
Are not there caught of the feeding mechanism etc?

(11) Others

The image is sometimes blocked, and the image stops.
The image is blocked when going to outer though it is normal in surroundings in the disk and the stopping symptom increases.

} There is a possibility with bad jitter value for such a symptom.

(12) CD During normal playback operation

a) Is TOC reading normal?
Displays total time for CD-DA.
Shifts to double-speed mode for V-CD.

↓ YES

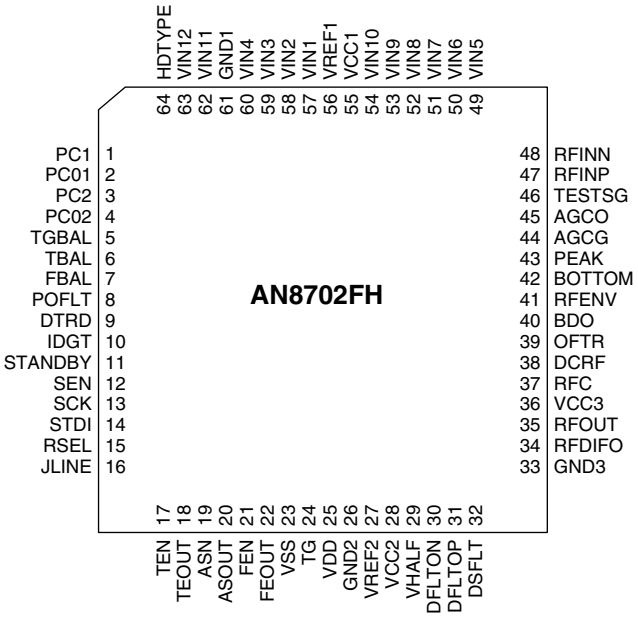
b)Playback possible? → NO

*--:-- is displayed during FL search.
According to [It is not possible to search] for DVD(9), check the feed and tracking systems.
*No sound is output although the time is displayed.(CA-DA)
DAC, etc, other than servo.
*The passage of time is not stable, or picture is abnormal.(V-CD)
*The wound of the disc and dirt are confirmed.

Description of major ICs

■ AN8702FH(IC101):Frontend processor

1.Pin layout

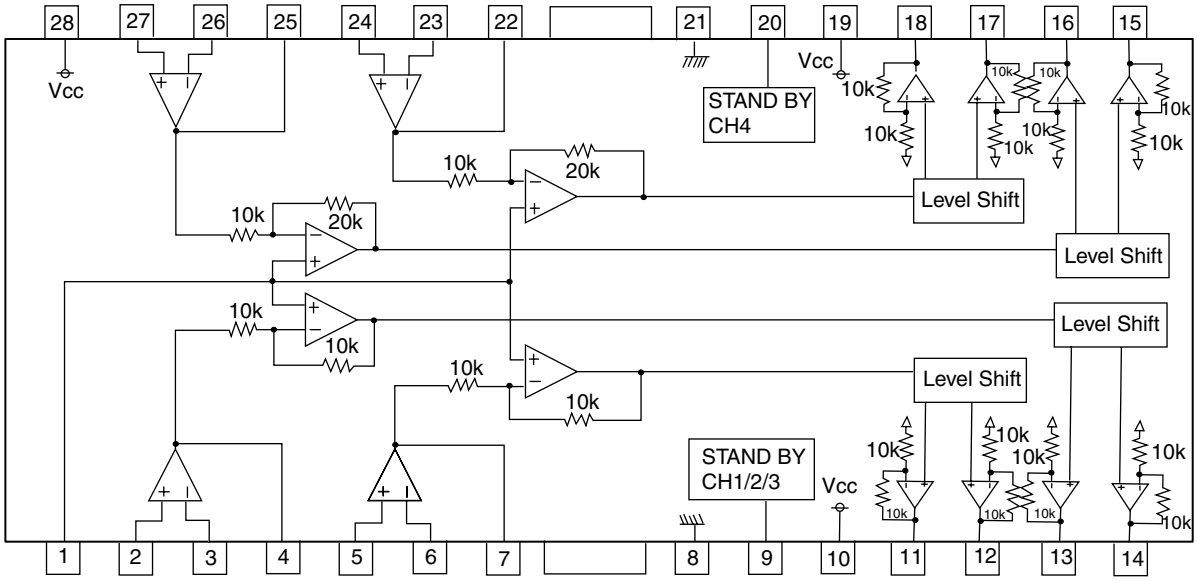


2.Pin function

Pin No.	Symbol	I/O	Description	Pin No.	Symbol	I/O	Description
1	PC1	I	Disc detection signal input (DVD)	34	RFDIFO		
2	PC01	I/O	Laser current control terminal	35	RFOUT	-	To TP101
3	PC2	I	Disc detection signal input (CD)	36	VCC3	-	Power supply terminal 5V
4	PC02	I/O	Laser current control terminal	37	RFC		
5	TGBAL	I	Tangential phase balance control terminal	38	DCRF	O	All addition amplifier capacitor terminal
6	TBAL	I	Tracking balance control terminal	39	OFTR	O	OFTR output terminal
7	FBAL	I	Focus balance control terminal	40	BDO	O	Drop out
8	POFLT	O	Track detection threshold level terminal	41	RFENV	O	RF envelope output terminal
9	DTRD	I	Data slice part data read signal input terminal	42	BOTTOM	O	Bottom envelope detection filter terminal
			(For RAM)	43	PEAK	O	Peak envelope detection filter terminal
10	IDGT	I	Data slice part address part gate signal input	44	AGCG	O	AGC amplifier gain control terminal
			terminal(For RAM)	45	AGCO		
11	STANDBY	I	Standby mode control terminal	46	TESTSG	I	TEST signal input terminal
12	SEN	I	SEN(Serial data input terminal)	47	RFINP	I	RF signal positive input terminal
13	SCK	I	SCK(Serial data input terminal)	48	RFINN	I	RF signal negative input terminal
14	STDI	I	STDI(Serial data input terminal)	49	VIN5	I	Focus input of external division into two terminal
15	RSEL			50	VIN6	I	Focus input of external division into two terminal
16	JLINE	I	J-line setting input(FEP)	51	VIN7	I	
17	TEN			52	VIN8	I	
18	TEOUT	O	Tracking error signal output terminal	53	VIN9	I	Focus input of external division into two terminal
19	ASN			54	VIN10	I	Focus input of external division into two terminal
20	ASOUT	O	Full adder signal output	55	VCC1	-	Power supply terminal 5V
21	FEN	I	Focus error output amplifier reversing input terminal	56	VREF1	O	VREF1 voltage output terminal
22	FEOUT	O	Focus error signal output terminal	57	VIN1	I	External division into four (DVD/CD) RF input
23	VSS	-	Connect to GND				terminal1
24	TG	O	Tangential phase error signal output terminal	58	VIN2	I	External division into four (DVD/CD) RF input
25	VDD	-	Power supply terminal 3V				terminal2
26	GND2	-	Connect to GND	59	VIN3	I	External division into four (DVD/CD) RF input
27	VREF2	O	VREF2 voltage output terminal				terminal3
28	VCC2	-	Power supply terminal 5V	60	VIN4	I	External division into four (DVD/CD) RF input
29	VHALF	O	VHALF voltage output terminal				terminal4
30	DFLTON	O	Equivalence RF-	61	GND1	-	Connect to GND
31	DFLTOP	O	Equivalence RF+	62	VIN11	I	Tracking input
32	DSFLT			63	VIN12	I	Tracking input
33	GND3	-	Connect to GND	64	HDTYPE	-	Connect to ground

■ BA5983FM-X (IC271) : 4CH DRIVER

1.Block diagram

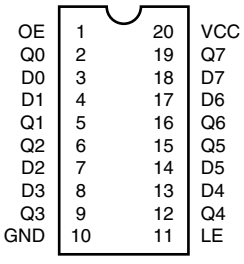


2.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BIAS IN	I	Input for Bias-amplifier	15	VO4(+)	O	Non inverted output of CH4
2	OPIN1(+)	I	Non inverting input for CH1 OP-AMP	16	VO4(-)	O	Inverted output of CH4
3	OPIN1(-)	I	Inverting input for CH1 OP-AMP	17	VO3(+)	O	Non inverted output of CH3
4	OPOUT1	O	Output for CH1 OP-AMP	18	VO3(-)	O	Inverted output of CH3
5	OPIN2(+)	I	Non inverting input for CH2 OP-AMP	19	PowVcc2	-	Vcc for CH3/4 power block
6	OPIN2(-)	I	Inverting input for CH2 OP-AMP	20	STBY2	I	Input for Ch4 stand by control
7	OPOUT2	O	Output for CH2 OP-AMP	21	GND	-	Substrate ground
8	GND	-	Substrate ground	22	OPOUT3	O	Output for CH3 OP-AMP
9	STBY1	I	Input for CH1/2/3 stand by control	23	OPIN3(-)	I	Inverting input for CH3 OP-AMP
10	PowVcc1	-	Vcc for CH1/2 power block	24	OPIN3(+)	I	Non inverting input for CH3 OP-AMP
11	VO2(-)	O	Inverted output of CH2	25	OPOUT4	O	Output for CH4 OP-AMP
12	VO2(+)	O	Non inverted output of CH2	26	OPIN4(-)	I	Inverting input for CH4 OP-AMP
13	VO1(-)	O	Inverted output of CH1	27	OPIN4(+)	I	Non inverting input for CH4 OP-AMP
14	VO1(+)	O	Non inverted output of CH1	28	PreVcc	-	Vcc for pre block

■ 74LCX373MTC-X(IC512,IC513)

1.Pin layout



2.Pin function

Symbol	Description
D0~D7	Data inputs
LE	Latch enable input
$\overline{OE}$	Output enable input
Q0~Q7	3-State latch outputs

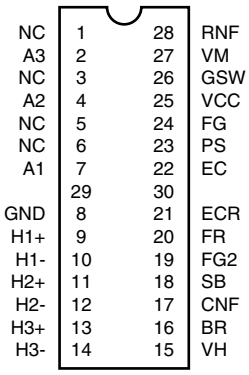
3.Truth table

INPUTS			OUTPUTS
LE	$\overline{OE}$	Dn	Qn
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	Q0

H = HIGH Voltage level
L = LOW Voltage level
Z = High impedance
X = Immaterial
Q0 = Previous Q0 before HIGH to LOW transition of latch enable

■ BA6664FM-X(IC251):Spindle motor driver

1.Pin layout

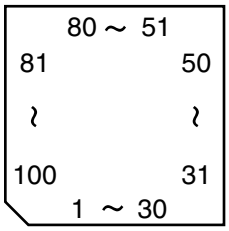


2.Pin function

Pin No.	Symbol	I/O	Description
1	NC	-	Non connect
2	A3	O	Output 3 for spindle motor
3	NC	-	Non connect
4	A2	O	Output 2 for spindle motor
5	NC	-	Non connect
6	NC	-	Non connect
7	A1	O	Output 1 for spindle motor
8	GND	-	Connect to ground
9	H1+	I	Positive input for hall input AMP 1
10	H1-	I	Negative input for hall input AMP 2
11	H2+	I	Positive input for hall input AMP 2
12	H2-	I	Negative input for hall input AMP 2
13	H3+	I	Positive input for hall input AMP 3
14	H3-	I	Negative input for hall input AMP 3
15	VH	I	Hall bias terminal
16	BR	-	Non connect
17	CNF	-	Capacitor connection pin for phase compensation
18	SB	O	Short brake terminal
19	FG2	-	Non connect
20	FR	-	Non connect
21	ECR	I	Torque control standard voltage input terminal
22	EC	I	Torque control voltage input terminal
23	PS	O	Start/stop switch (power save terminal)
24	FG	O	FG signal output terminal
25	VCC	-	Power supply for signal division
26	GSW	O	Gain switch
27	VM	-	Power supply for driver division
28	RNF	O	Resistance connection pin for output current sense
29		-	Connect to ground
30		-	Connect to ground

■ JCV8005-2(IC701):CPPM (Content protection for pre-recorded media)

1.Pin layout



2.Pin function

JCV8005-2 1/2

Pin No.	Symbol	I/O	Description
1	VDD	-	Power supply
2	GND	-	Connect to ground
3~10	HDATA0~7	I/O	Data input/output terminal (both by 8 bits)
11	VDD	-	Power supply
12	GND	-	Connect to ground
13~20	HADDR0~7	I	8 bit address bus to internal address (connect to host)
21	VDD	-	Power supply
22	GND	-	Connect to ground
23	NCS	I	Chip select signal from host
24	NRD	I	Data read signal from host
25	NWR	I	Data write signal from host
26	NIRQ	O	Interrupt of request to host
27	WAIT	O	Wait demand to host
28	NRESET	I	Reset signal from host
29	VDD	-	Power supply
30	GND	-	Connect to ground
31	VDD	-	Power supply
32	GND	-	Connect to ground
33~36	STD7~4_OUT	O	Data output to DVD decoder (8 bits)
37	GND	-	Connect to ground
38~41	STD3~0_OUT	O	Data output to DVD decoder (8 bits)
42	VDD	-	Power supply
43	GND	-	Connect to ground
44	REQ_IN	I	Request signal for forwarding control by decoder
45	DACK_OUT	O	Output signal to decoder which shows effective data
46	STCLK_OUT	O	Data strobe signal to decoder
47	SYNC_OUT	O	Sector sink signal to decoder
48	STERROUT	-	Non connect
49	VDD	-	Power supply
50	GND	-	Connect to ground
51	VDD	-	Power supply
52	GND	-	Connect to ground
53	NG_RD	I	Glue logic input signal from host
54	NG_WR	I	Glue logic input signal from host
55	G_WITODC	I	Glue logic input signal from front end
56	G_CSDEC	I	Glue logic input signal from host
57	G_WITDEC	I	Glue logic input signal from decoder
58	VDD	-	Power supply

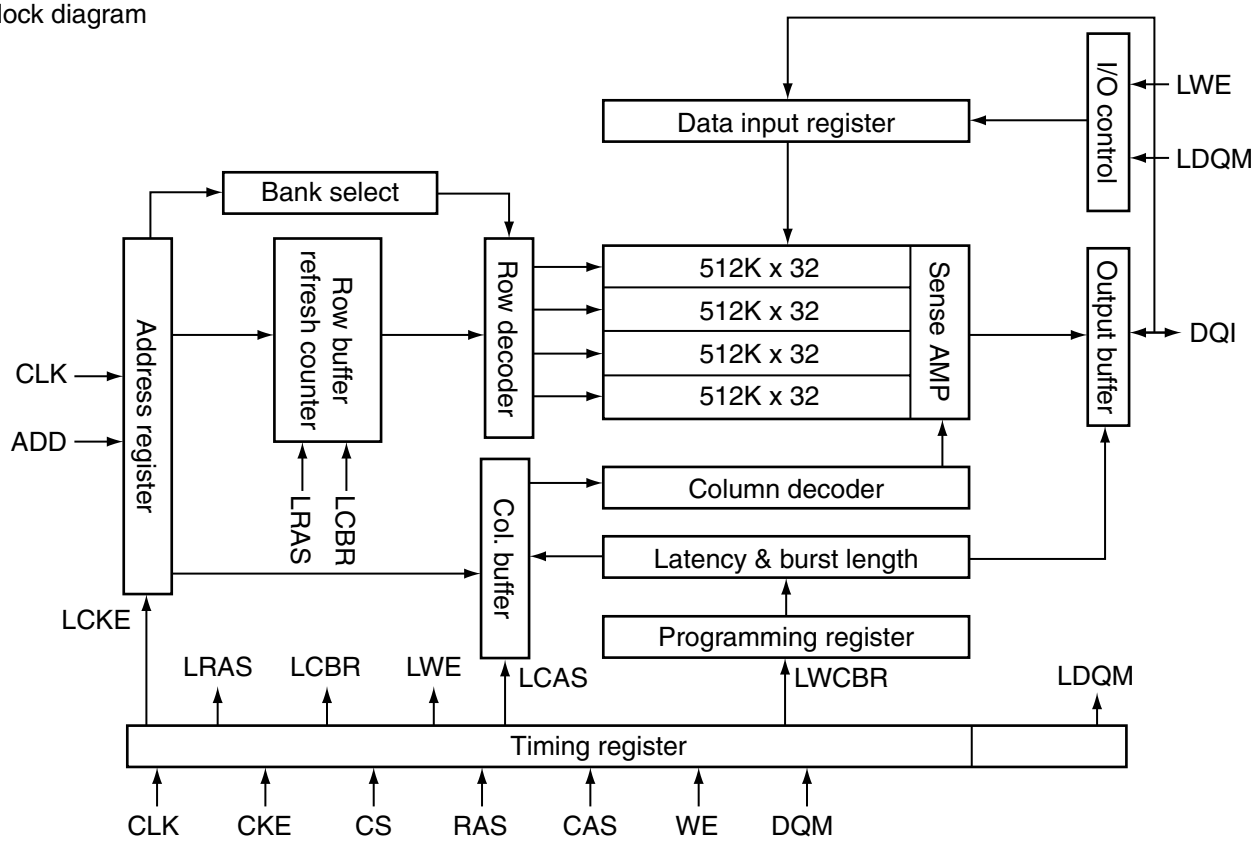
2.Pin function

JCV8005-2 2/2

Pin No.	Symbol	I/O	Description
59	GND	-	Connect to ground
60	WAIT1	O	Glue logic output signal to host
61	WAIT2	-	Non connect
62	WAITIN	I	Glue logic input signal (connect to 27 pin)
63	VDD	-	Power supply
64	GND	-	Connect to ground
65	TEST_IN	I	Connect to ground
66,67	NC	-	Non connect
68	VDD	-	Power supply
69	GND	-	Connect to ground
70	CLKOCTL	I	Input terminal for crystal-oscillator circuit on/off control
71	NC	-	Non connect
72	OSCI	I	Crystal oscillation terminal (input side)
73	OSCO	O	Crystal oscillation terminal (output side)
74	NC	-	Non connect
75	VDD	-	Power supply
76	GND	-	Connect to ground
77	33OUT	O	Oscillation output terminal
78	16OUT	O	Oscillation output terminal
79	VDD	-	Power supply
80	GND	-	Connect to ground
81	VDD	-	Power supply
82	GND	-	Connect to ground
83	STERR_IN	I	Presence of data error from front end
84	SYNC_IN	I	Sector sink signal from front end
85	STCLK_IN	I	Data clock signal from front end
86	DACK_IN	I	Signal which shows effective data from front end
87	REQ_OUT	O	Request signal for forwarding control to front end
88	VDD	-	Power supply
89	GND	-	Connect to ground
90~93	STD0~3_IN	I	Data input from front end (8 bits)
94	GND	-	Connect to ground
95~98	STD4~7_IN	I	Data input from front end (8 bits)
99	VDD	-	Power supply
100	GND	-	Connect to ground

■ K4S643232E-TC70(IC505):DRAM

1.Block diagram



2.Pin function

Symbol	Description	Symbol	Description
CLK	System clock signal input	DQM0~3	Data input/output mask
CS	Chip select input	DQ0~31	Data input/output
CKE	Clock enable	VDD	Power supply terminal
A0~A10	Address	VSS	Connect to ground
BA0,1	Bank select address	VDDQ	Power supply terminal
RAS	Row address strobe	VSSQ	Connect to ground
CAS	Column address strobe	NC	Non connect
WE	Write enable		

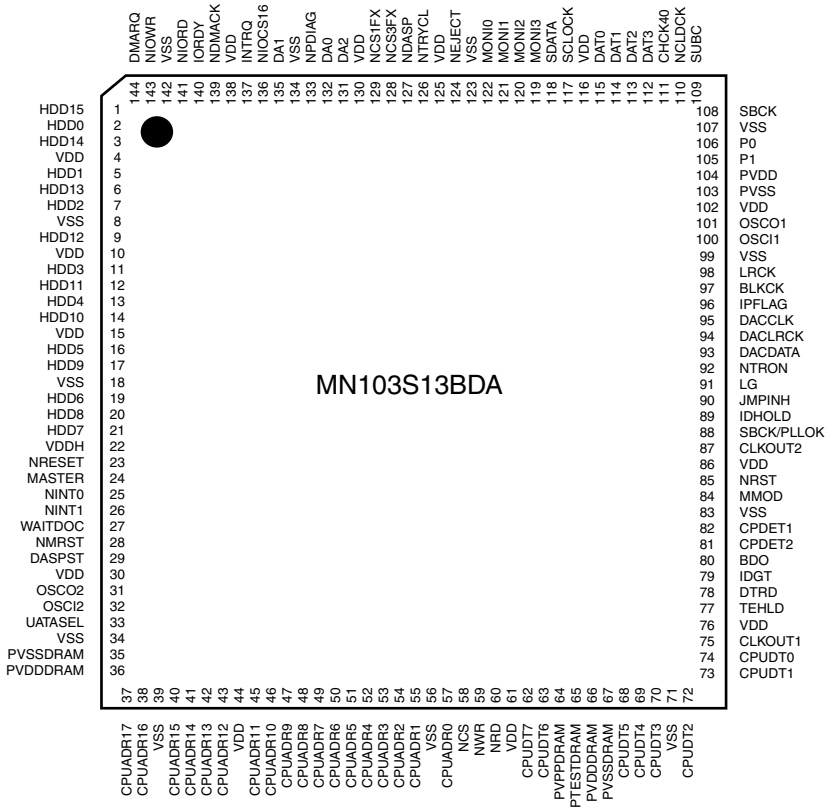
■ MN102L25GGT3(IC401):Unit CPU

Pin function

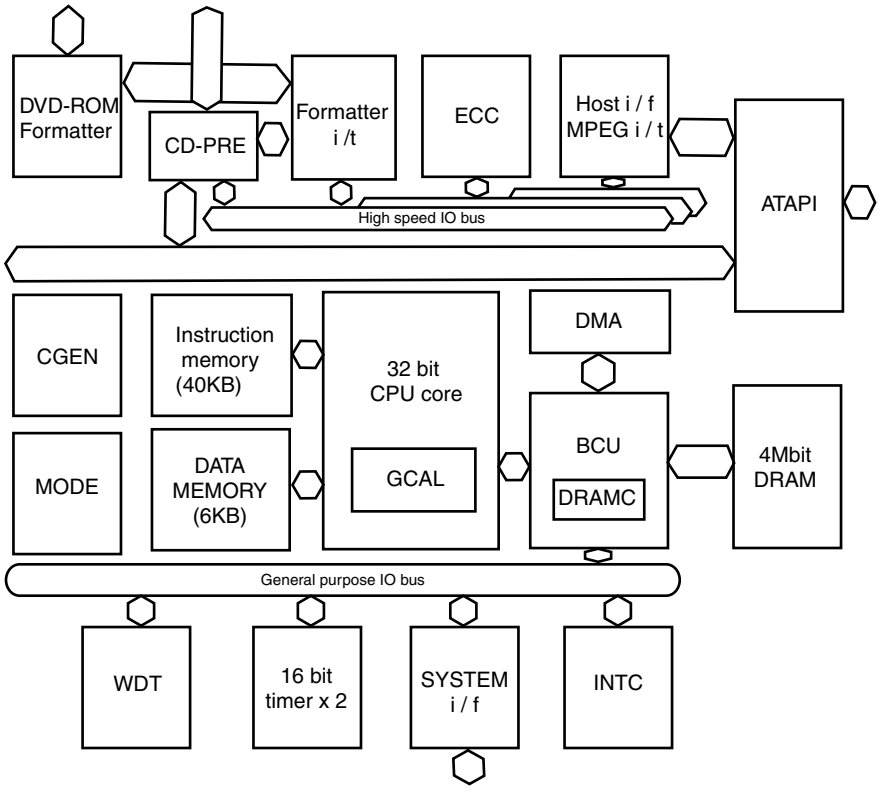
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	SWUPDN	I	Elevator UP/DOWN switch detect
2	RE	O	Read enable	52	SWOPEN	I	Tray OPEN/CLOSE switch detect
3	SPMUTE	O	Spindle muting output to IC251	53	ADSCEN	O	Serial enable signal for ADSC
4	WEN	O	Write enable	54	VDD	-	Power supply
5	LMMUTE	O	Loading motor standby control	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for CPPM	57	BUSY	-	Non connect
8	CS3	-	Non connect	58	REQ	O	Communication Request
9	DRVMUTE	O	Driver mute	59	CIRCEN	O	CIRC command select
10	SPKICK	O	Spin kick (Non connect)	60	-	-	Non connect
11	LSIRST	O	LSI reset	61	VSS	-	Ground
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLKO	I	Communication clock
18	SYSCLK	-	Connect to TP169	68	S2UDT	I	Communication input data
19	VSS	-	Ground	69	U2SDT	O	Communication output data
20	XI	-	Not use (Connect to vss)	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Connect to TP170	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input	73	-	-	Not use
24	OSCO	O	Clock signal output	74	-	-	Not use
25	MODE	I	CPU Mode selection input	75	NMI	-	Not use
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	CSSIRQ	-	Not use
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Interruption of system control
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	-	Non connect	91	TEST8	I	Test signal 8 input
42	A19	-	Non connect	92	VSS	-	Ground
43	VSS	-	Ground	93	D0	I/O	Data bus 0 of CPU
44	A20	-	Non connect	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	-	Connect to TP910	95	D2	I/O	Data bus 2 of CPU
46	HAGUP	O		96	D3	I/O	Data bus 3 of CPU
47	TCLOSE	I/O	Tray close signal	97	D4	I/O	Data bus 4 of CPU
48	TOPEN	I/O	Tray open signal	98	D5	I/O	Data bus 5 of CPU
49	HMFON			99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ MN103S13BDA(IC301):Optical disc controller

1.Pin layout



2.Block diagram



3.Pin function (1/3)

Pin No.	Symbol	I/O	Description
1	HDD15	I/O	ATAPI Data
2	HDD0	I/O	ATAPI Data
3	HDD14	I/O	ATAPI Data
4	VDD	-	Power supply 3V
5	HDD1	I/O	ATAPI Data
6	HDD13	I/O	ATAPI Data
7	HDD2	I/O	ATAPI Data
8	VSS	-	Connect to GND
9	HDD12	I/O	ATAPI Data
10	VDD	-	Power supply 2.7V
11	HDD3	I/O	ATAPI Data
12	HDD11	I/O	ATAPI Data
13	HDD4	I/O	ATAPI Data
14	HDD10	I/O	ATAPI Data
15	VDD	-	Power supply 3V
16	HDD5	I/O	ATAPI Data
17	HDD9	I/O	ATAPI Data
18	VSS	-	Connect to GND
19	HDD6	I/O	ATAPI Data
20	HDD8	I/O	ATAPI Data
21	HDD7	I/O	ATAPI Data
22	VDDH		
23	NRESET	I	ATAPI Reset input
24	MASTER	I/O	ATAPI Master/slave select
25	NINT0	O	Interruption of system control 0
26	NINT1	O	Interruption of system control 1
27	WAITDOC	O	Wait control of system control
28	NMRST	O	Reset of system control (Connect to TP302)
29	DASPST	I	Setting of initial value of DASP signal
30	VDD	-	Power supply 3V
31	OSCO2	O	Non connect
32	OSCI2	I	Non connect
33	UATASEL	I	Connect to VSS
34	VSS	-	Connect to GND
35	PVSSDRAM		Connect to VSS
36	PVDDDRAM		Connect to VDD(2.7V)
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS	-	Connect to GND
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD	-	Power supply 2.7V
45	CPUADR11	I	System control address
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address

3.Pin function (2/3)

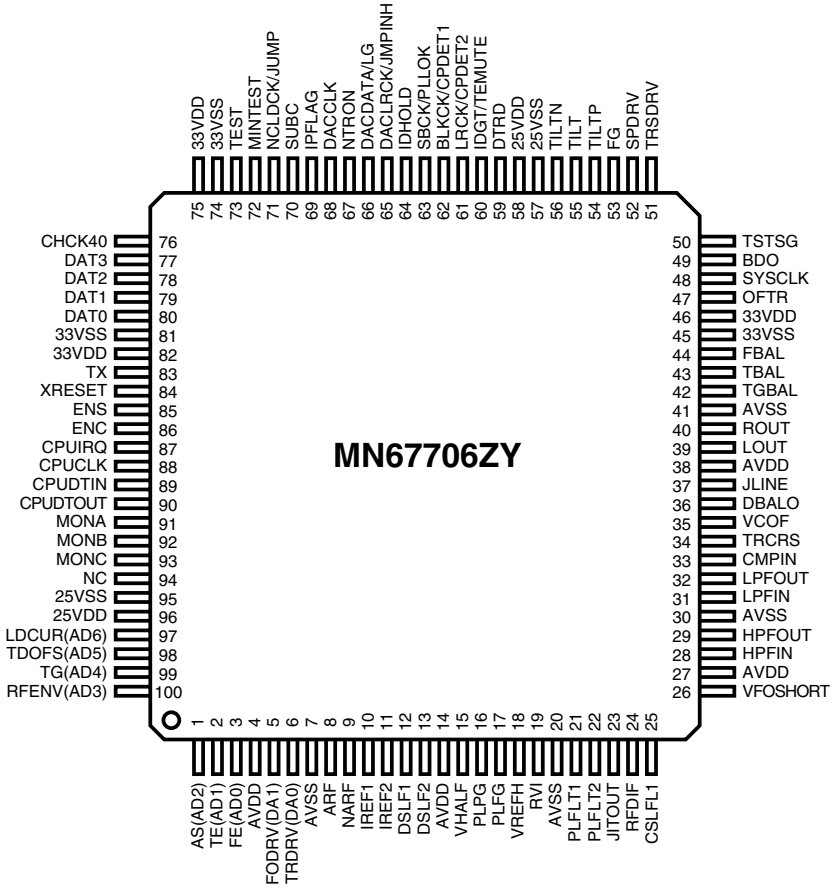
Pin No.	Symbol	I/O	Description
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS	-	Connect to GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip select
59	NWR	I	Writing system control
60	NRD	I	Reading system control
61	VDD	-	Power supply 3V
62	CPUDT7	I/O	System control data
63	CPUDT6	I/O	System control data
64	PVPPDRAM	O	Connect to VSS
65	PTESTDRAM	I	Connect to VSS
66	PVDDDRAM		Connect to VDD(2.7V)
67	PVSSDRAM		Connect to VSS
68	CPUDT5	I/O	System control data
69	CPUDT4	I/O	System control data
70	CPUDT3	I/O	System control data
71	VSS	-	Connect to GND
72	CPUDT2	I/O	System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	Clock signal output (16.9/11.2/8.45MHz)
76	VDD	-	Power supply 3V
77	TEHLD	O	Mirror gate (Connect to TP141)
78	DTRD	O	Data frequency control switch (Connect to TP304)
79	IDGT	O	CAPA switch
80	BDO	I	RF Dropout/BCA data
81	CPDET2	I	Outer capacity detection
82	CPDET1	I	Inner capacity detection
83	VSS	-	Connect to GND
84	MMOD	I	Connect to VSS
85	NRST	I	System reset
86	VDD	-	Power supply 3V
87	CLKOUT2	O	Clock 16.9MHz
88	SBCK/PLLOK	O	Flame mark detection
89	IDOHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition
91	LG	O	Land/group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Serial data output (Connect to TP148)
94	DACLRCK	O	Identification signal of L and R (Connect to TP149)
95	DACCLK	I	Clock for serial data output
96	IPFLAG	I	Input of IP flag
97	BLKCK	I	Sub code/block/input clock
98	LRCK	I	Identification signal of L and R (Connect to VSS)
99	VSS	-	Connect to GND
100	OSCI1	I	Oscillation input terminal 16.9MHz

3.Pin function (3/3)

Pin No.	Symbol	I/O	Description
101	OSCO1	O	Oscillation output terminal 16.9MHz
102	VDD	-	Power supply 3V
103	PVSS	-	Connect to GND
104	PVDD	-	Power supply 3V
105	P1	I/O	Terminal master polarity switch input
106	P0	I/O	CIRC-RAM,OVER/UNDER Interruption
107	VSS	-	Connect to GND
108	SBCK	O	Clock output for sub code,serial input
109	SUBC	I	Sub code,serial input
110	NCLDCK	I	Sub code,flame clock input
111	CHCK40	I	Clock is read to DAT3~0 (Output of division frequency from ADSC)
112	DAT3	I	Data is read from disc (Going side by side output from ADSC)
113	DAT2	I	Data is read from disc (Going side by side output from ADSC)
114	DAT1	I	Data is read from disc (Going side by side output from ADSC)
115	DAT0	I	Data is read from disc (Going side by side output from ADSC)
116	VDD	-	Power supply 3V
117	SCLOCK	I/O	Debug serial clock (270 ohm pull up)
118	SDATA	I/O	Debug serial data (270 ohm pull up)
119	MONI3	O	Internal good title monitor (Connect to TP150)
120	MONI2	O	Internal good title monitor (Connect to TP151)
121	MONI1	O	Internal good title monitor (Connect to TP152)
122	MONI0	O	Internal good title monitor (Connect to TP153)
123	VSS	-	Connect to GND
124	NEJECT	I	Eject detection
125	VDD	-	Power supply 2.7V
126	NTRYCL	I	Non connect (Tray close detection)
127	NDASP	I/O	ATAPI drive active / slave connect I/O
128	NCS3FX	I	Non connect (ATAPI host chip select)
129	NCS1FX	I	Non connect (ATAPI host chip select)
130	VDD	-	Power supply 3V
131	DA2	I/O	ATAPI host address
132	DA0	I/O	Non connect (ATAPI host address)
133	NPDIAG	I/O	ATAPI Slave master diagnosis input
134	VSS	-	Connect to GND
135	DA1	I/O	Non connect (ATAPI host address)
136	NIOCS16	O	Output of selection of width of ATAPI host data bus
137	INTRQ	O	ATAPI Host interruption output
138	VDD	-	Power supply 3V
139	NDMACK	I	Non connect (ATAPI Host DMA characteristic)
140	IORDY	O	ATAPI Host ready output (Connect to TP157)
141	NIORD	I	Non connect (ATAPI host read)
142	VSS	-	Connect to GND
143	NIOWR	I/O	ATAPI Host write
144	DMARQ	O	ATAPI Host DMA request (Connect to TP159)

■ MN67706ZY (IC201) : Auto digital servo controller

1.Pin layout



2.Pin functions (1/3)

Pin No.	Symbol	I/O	Description
1	AS(AD2)	I	AS : Full adder signal(FEP)
2	TE(AD1)	I	Phase difference/3 beam tracking error(FEP)
3	FE(AD0)	I	Focus error(FEP)
4	AVDD	-	Apply 3.3V(For analog circuit)
5	FODRV(DA1)	O	Focus drive(DRVIC)
6	TRDRV(DA0)	O	Tracking drive(DRVIC)
7	AVSS	-	Ground(For analog circuit)
8	ARF	I	Equivalence RF+(FEP)
9	NARF	I	Equivalence RF-(FEP)
10	IREF1	I	Reference current1(For DBAL)
11	IREF2	I	Reference current2(For DBAL)
12	DSLF1	I/O	Connect to capacitor1 for DSL
13	DSLF2	I/O	Connect to capacitor2 for DSL
14	AVDD	-	Apply 3.3V(For analog circuit)
15	VHALF	I	Reference voltage 1.65+-0.1V(FEP)
16	PLPG	-	Not use(PLL phase gain setting resistor terminal)
17	PLFG	-	Not use(PLL frequency gain setting resistor terminal)
18	VREFH	I	Reference voltage 2.2V+-0.1V(FEP)
19	RVI	I/O	Connect to resistor for VREFH reference current source
20	AVSS	-	Ground(For analog circuit)
21	PLFLT1	O	Connect to capacitor1 for PLL
22	PLFLT2	O	Connect to capacitor2 for PLL
23	JITOUT	I/O	Output for jitter signal monitor
24	RFDIF	I	Not use
25	CSLFL1	I/O	Pull-up to VHALF

2.Pin function (2/3)

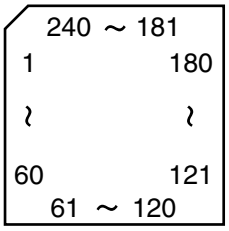
Pin No.	Symbol	I/O	Description
26	VFOSHORT	O	VFO short output
27	AVDD	-	Apply 3.3V(For analog circuit)
28	HPFIN	I	Pull-up to VHALF
29	HPFOUT	O	Connect to TP208
30	AVSS	-	Ground(For analog circuit)
31	LPFIN	I	Pull-up to VHALF
32	LPFOUT	O	Not use
33	CMPIN	I	Connect to TP210
34	TRCRS	I	Input signal for track cross formation
35	VCOF	I/O	JFVCO control voltage
36	DBALO	O	DSL balance adjust output
37	JLINE	O	J-line setting output(FEP)
38	AVDD	-	Apply 3.3V(For analog circuit)
39	LOUT	O	Connect to TP203 (Analog audio left output)
40	ROUT	O	Connect to TP204 (Analog audio right output)
41	AVSS	-	Ground(For analog circuit)
42	TGBAL	O	Tangential balance adjust(FEP)
43	TBAL	O	Tracking balance adjust(FEP)
44	FBAL	O	Focus balance adjust(FEP)
45	33VSS	-	Ground(For I/O)
46	33VDD	-	Apply 3.3V(For I/O)
47	OFTR	I	Off track signal
48	SYSCLK	I	16.9344MHz system clock input(ODC)
49	BDO	I	Drop out(FEP)
50	TSTSG	O	Calibration signal(FEP)
51	TRSDRV	O	Traverse drive(DRVIC)
52	SPDRV	O	Spindle drive output(DRVIC)
53	FG	I	FG signal input (Spindle motor driver)
54	TILTP	O	Connect to TP205
55	TILT	O	Connect to TP206
56	TILTN	O	Connect to TP207
57	25VSS	-	Ground(For internal core)
58	25VDD	-	Apply 2.5V(For internal core)
59	DTRD	I	Data read control signal(ODC)
60	IDGT/TEMUTE	I	Pull-down to Ground
61	LRCK/CPDET2	O	LR channel data strobe(ODC)/
62	BLKCK/CPDET1	O	CD sub code synchronous signal(ODC)/
63	SBCK/PLLOK	I	CD sub code data shift clock(ODC)/PLL pull-in OK signal input
64	IDHOLD	I	Pull-down to Ground
65	DACLRCK/JMPINH	I	1bit DAC-LR channel data strobe(ODC)/
66	DACDATA/LG	I	CD 1bit DAC channel data(ODC)
67	NTRON	O	L : Tracking ON(ODC)
68	DACCLK	O	1bit DAC channel data shift clock(ODC)
69	IPFLAG	O	CIRC error flag(ODC)
70	SUBC	O	CD sub code(ODC)
71	NCLDCK/JUMP	O	CD sub code data frame clock(ODC)/DVD JUMP signal(ODC)
72	MINTEST	I	Pull-down to Ground(For MINTEST)
73	TEST	I	Pull-down to Ground(For TEST)
74	33VSS	-	Ground(For I/O)
75	33VDD	-	Apply 3.3V(For I/O)
76	CHCK40	O	Clock for SRDATA(ODC)
77	DAT3	O	SRDATA3(ODC)
78	DAT2	O	SRDATA2(ODC)
79	DAT1	O	SRDATA1(ODC)
80	DAT0	O	SRDATA0(ODC)

2.Pin function (3/3)

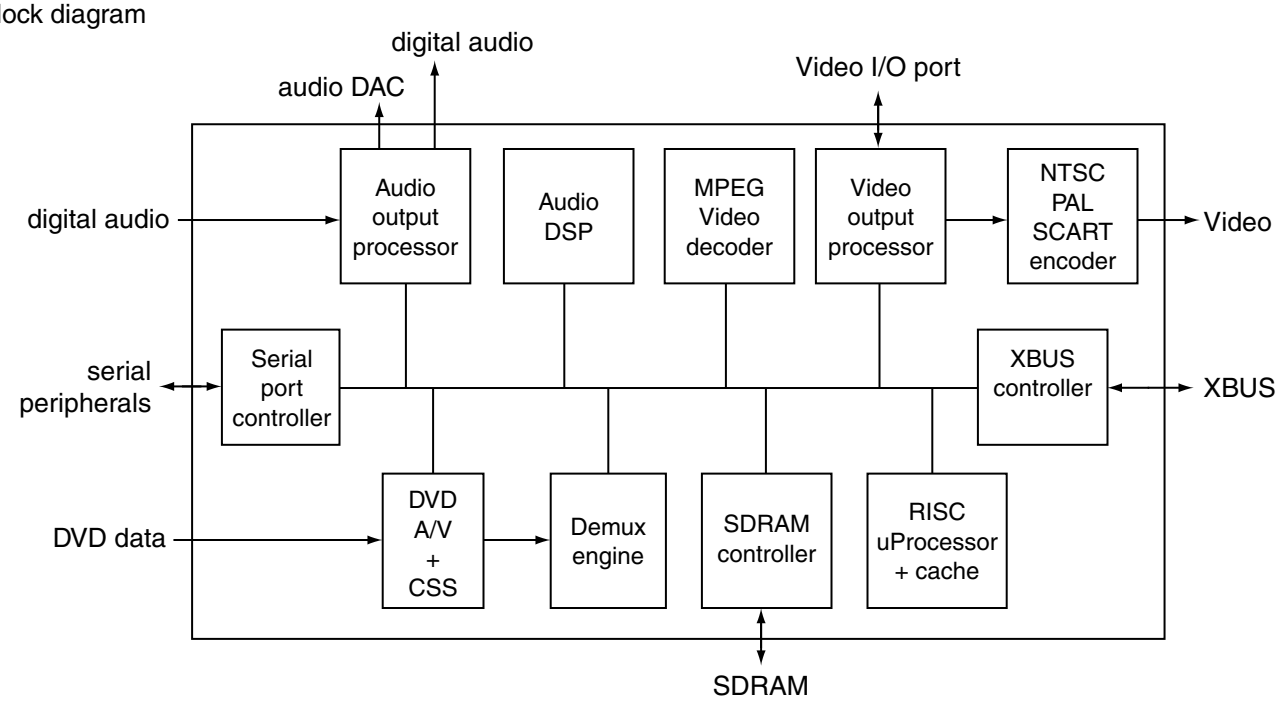
Pin No.	Symbol	I/O	Description
81	33VSS	-	Ground(For I/O)
82	33VDD	-	Apply 3.3V(For I/O)
83	TX	O	Digital audio interface
84	XRESET	I	Reset input (System control)
85	ENS	I	Servo DSC serial I/F chip select (System control)
86	ENC	I	CIRC serial I/F chip select (System control)
87	CPUIRQ	O	Interrupt request (System control)
88	CPUCLK	I	Syscon serial I/F clock (System control)
89	CPUDTIN	I	Syscon serial I/F data input (System control)
90	CPUDTOUT	O	Syscon serial I/F data output (System control)
91	MONA	O	Connect to TP226 (Monitor terminal A)
92	MONB	O	Connect to TP225 (Monitor terminal A)
93	MONC	O	Connect to TP224 (Monitor terminal A)
94	NC	O	Connect to TP211
95	25VSS	-	Ground(For internal core)
96	25VDD	-	Apply 2.5V(For internal core)
97	LDCUR(AD6)	I	
98	TDOFS(AD5)	I	
99	TG(AD4)	I	Tangential phase difference(FEP)
100	RFENV(AD3)	I	RF envelope input(FEP)

■ NDV8601VWA-BB(IC501):AV Decoder

1.Pin layout



2.Block diagram



3.Pin function (1/4)

Pin No.	Symbol	I/O	Description
1	VDDio	-	Power supply terminal 3.3V
2,3	MD10,11	I/O	SDRAM Data bus terminal
4	VDD	-	Power supply terminal 1.8V
5	MD12	I/O	SDRAM Data bus terminal
6	VSSio	-	Connect to ground
7~9	MD13~15	I/O	SDRAM Data bus terminal
10	VDDio	-	Power supply terminal 3.3V
11	DQM1	O	SDRAM Data byte enable
12,13	MA9,8	O	SDRAM Address bus terminal
14	VSSio	-	Connect to ground
15,16	MA7,6	O	SDRAM Address bus terminal
17	VSS	-	Connect to ground
18	MA5	O	SDRAM Address bus terminal
19	VDDio	-	Power supply terminal 3.3V
20,21	MA4,3	O	SDRAM Address bus terminal
22	MCLK	O	SDRAM Clock output
23	VSSio	-	Connect to ground
24	CKE	O	SDRAM Clock enable output
25,26	MA2,1	O	SDRAM Address bus terminal
27	VDDio	-	Power supply terminal 3.3V
28	MA0	O	SDRAM Address bus terminal
29	MA10	O	SDRAM Address bus terminal

3.Pin function (NDV8601VWA-BB 2/4)

Pin No.	Symbol	I/O	Description
30	MA11	-	Non connect
31	VSSio	-	Connect to ground
32,33	MA12,13	O	SDRAM Address bus, reserved for terminal compatibility with 64Mb SDRAM
34	VDD	-	Power supply terminal 1.8V
35	CS0	O	SDRAM Primary bank chip select
36	VDDio	-	Power supply terminal 3.3V
37	RAS	O	SDRAM Command bit
38	CAS	O	SDRAM Command bit
39	WE	O	SDRAM Command bit
40	VSSio	-	Connect to ground
41	DQM0	O	SDRAM Data byte enable
42	DQM2	O	SDRAM Data byte enable
43	MD16	I/O	SDRAM Data bus terminal
44	VDDio	-	Power supply terminal 3.3V
45,46	MD17,18	I/O	SDRAM Data bus terminal
47	VSS	-	Connect to ground
48	MD19	I/O	SDRAM Data bus terminal
49	VSSio	-	Connect to ground
50~52	MD20~22	I/O	SDRAM Data bus terminal
53	VDDio	-	Power supply terminal 3.3V
54~56	MD23~25	I/O	SDRAM Data bus terminal
57	VSSio	-	Connect to ground
58~61	MD26~29	I/O	SDRAM Data bus terminal
62	VDDio	-	Power supply terminal 3.3V
63,64	MD30,31	I/O	SDRAM Data bus terminal
65	DQM3	O	SDRAM Data byte enable
66	CS1	O	SDRAM Extension bank chip select
67	VSSD	-	Connect to ground
68	SPDIF	O	S/PDIF Digital audio output terminal
69	VSSio	-	Connect to ground
70	AIN	I	Digital audio input for digital micro; can be used as GPIO
71	AOUT3	O	Serial audio output data to audio DAC for left and right channels for down-mix
72	AOUT2	O	Serial audio output data to audio DAC for surround left and right channels
73	AOUT1	O	Serial audio output data to audio DAC for center and LFE channels
74	AOUT0	O	Serial audio output data to audio DAC for left and right channels
75	VDDio	-	Power supply terminal 3.3V
76	PCMCLK	O	Audio DAC PCM sampling clock frequency, common clock for DACs and ADC
77	VDD	-	Power supply terminal 1.8V
78	ACLK	O	Audio interface serial data clock, common clock for DACs and AD converter
79	LRCLK	O	Left / right channel clock, common clock for DACs and ADC
80	SRST	O	Active low RESET signal for peripheral reset
81	RSTP	I	RESET_Power : from system, used to reset frequency synthesizer and rest of chip
82	VSSio	-	Connect to ground
83	RXD1	I	UART1 Serial data input from external serial device, used for IR receiver
84	SSPIN1	I/O	SSP1 Data in or 16X clock for USART function in UART1
85	VSS	-	Connect to ground
86	SSPOUT1	I/O	SSP1 Data out or UART1 data-terminal-ready signal
87	SSPCLK1	I/O	SSP1 Clock or UART1 clear-to -send signal
88	SSPCLK0	I/O	SSP0 Clock or request-to-send function in UART1
89	VDD	-	Power supply terminal 1.8V
90	SSPIN0	I/O	SSP0 Data in or 16X clock for USART function in UART0

3.Pin function (NDV8601VWA-BB 3/4)

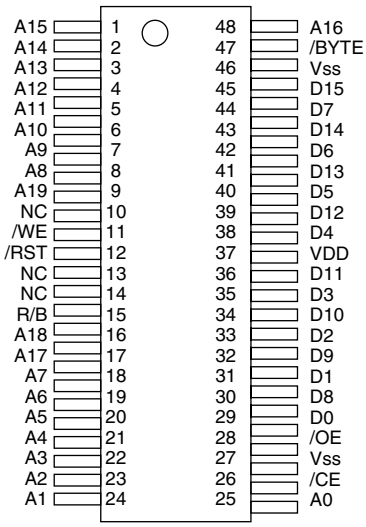
Pin No.	Symbol	I/O	Description
91	VDDio	-	Power supply terminal 3.3V
92	SSPOUT0	I/O	SSP0 Data out or UART0 data-terminal-ready signal
93	TXD0	I/O	UART0 Serial data output to an external serial device
94	RXD0	I	UART0 Serial data input from external serial device
95	CTS0	I/O	UART0 Clear-to-send signal
96	RTS0	I/O	UART0 Request-to-send signal
97	VSSio	-	Connect to ground
98	CXI	I	Crystal input terminal for on-chip oscillator or system input clock
99	CXO	O	Crystal output terminal for on-chip oscillator
100	OSCVSS	-	Connect to ground for oscillator
101	OSCVDD	-	Power supply terminal for oscillator 1.8V
102	MVCKVDD	-	Power supply terminal for main and video clock PLL 3.3V
103	SCEN	I	Scan chain test enable
104	MVCKVSS	-	Connect to ground for main and video clock PLL
105	ACLKVSS	-	Connect to ground for audio clock PLL
106	SCMD	I	Scan chain test mode
107	ACLKVDD	-	Power supply terminal for audio clock PLL 3.3V
108	VDDDAK	-	Power supply terminal for DAC digital 1.8V
109	VSSDAC	-	Connect to ground for DAC digital
110	Cr/R	O	Video signal output (Cr output : composite/component Red output)
111	IOM	O	Cascaded DAC differential output used to dump current into external resistor for power
112	C/Cb/B	O	Video signal output (Chrominance output for NTSC/PAL S-Video Cb output for component Blue output)
113	VAA3	-	Power supply terminal for DAC analog 3.3V
114	Y/G	O	Video signal output (Luminance for S-Video and component Green output)
115	VSSA	-	Connect to ground for DAC analog
116	VREF	-	Non connect
117	VAA	-	
118	CVBS/C	O	Video signal output (Composite video Chrominance output for S-Video)
119	RSET	O	Current setting resistor of output DACs
120	COMP	O	Compensation capacitor connection
121	VSS	-	Connect to ground
122	VCLK	-	Non connect
123	VSYNC	-	Non connect
124	HSYNC	-	Non connect
125	VDDio	-	Power supply terminal 3.3V
126~131	VI07~02	-	Non connect
132	VSSio	-	Connect to ground
133,134	VI01,00	-	Non connect
135	VDD	-	Power supply terminal 1.8V
136~139	AD31~28	I/O	Multiplexed address / data bus terminal
140	VDDio	-	Power supply terminal
141~144	AD27~24	I/O	Multiplexed address / data bus terminal
145	PWE3	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
146	AD23	I/O	Multiplexed address / data bus terminal
147	VSSio	-	Connect to ground
148~153	AD22~17	I/O	Multiplexed address / data bus terminal
154	VDDio	-	Power supply terminal 3.3V
155	AD16	I/O	Multiplexed address / data bus terminal
156	PWE2	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
157,158	AD15,14	I/O	Multiplexed address / data bus terminal
159	VDD	-	Power supply terminal 1.8V

3.Pin function (NDV8601VWA-BB 4/4)

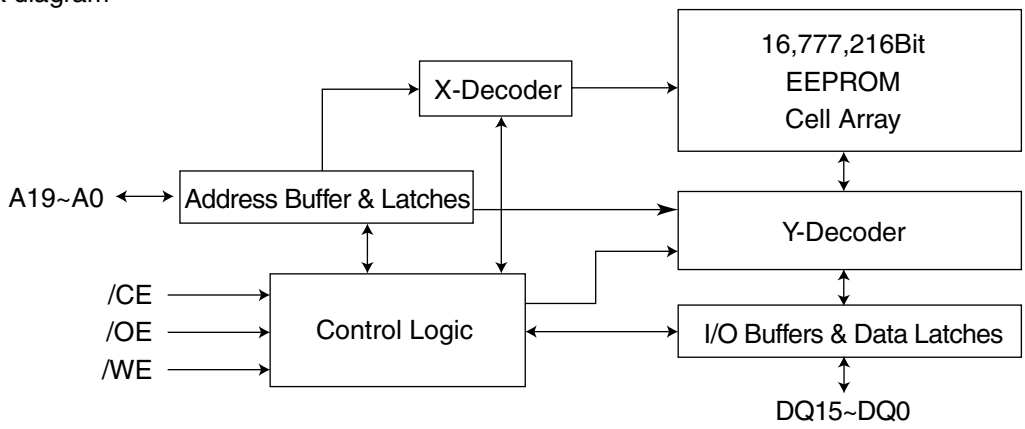
Pin No.	Symbol	I/O	Description
160	SCLK	O	External bus clock used for programmable host peripherals
161	ACK	I/O	Programmable WAIT/ACK/RDY control
162	VSSio	-	Connect to ground
163~168	AD13~8	I/O	Multiplexed address / data bus terminal
169	VDDio	-	Power supply terminal 3.3V
170	PWE1	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
171	VSS	-	Connect to ground
172~176	AD7~3	I/O	Multiplexed address / data bus terminal
177	VSSio	-	Connect to ground
178~180	AD2~0	I/O	Multiplexed address / data bus terminal
181	VDDio	-	Power supply terminal 3.3V
182	PWE0	I/O	Byte write enable for FLASH,EEPROM,SRAM or peripherals terminal
183	ALE	I/O	Address latch enable
184~187	LA0~3	I/O	Latched address 0~3
188	VSSio	-	Connect to ground
189	RD	I/O	Read terminal
190	LHLDA	O	Bus hold acknowledge in slave mode
191	LHLD	I	Bus hold request from external master in slave mode
192	VDD	-	Power supply terminal 1.8V
193	PCS0	O	Peripheral chip select 0, generally used for enabling the program store ROM/FLASH
194,195	XI01,02	I/O	Programmable general purpose external input/output
196	VDDio	-	Power supply terminal 3.3V
197~200	XI03~06	I/O	Programmable general purpose external input/output
201	VSS	-	Connect to ground
202,203	XI07,08	I/O	Programmable general purpose external input/output
204	VSSio	-	Connect to ground
205	XI09	I/O	Programmable general purpose external input/output
206~209	XID10~13	I/O	Programmable general purpose external input/output
210	VDDio	-	Power supply terminal 3.3V
211	XID14	I/O	Programmable general purpose external input/output
212	VDD	-	Power supply terminal 1.8V
213	DSYNC	I	DVD Parallel mode sector sync
214	DREQ	O	DVD Parallel mode data request
215	DCLK	I	Data sampling clock
216	DSTB	I	Parallel mode data valid, serial mode left/right clock
217	DVD0	I	DVD Drive parallel data port
218	VSSio	-	Connect to ground
219~223	DVD1~5	I	DVD Drive parallel data port
224	VDDio	-	Power supply terminal 3.3V
225,226	DVD6,7	I	DVD Drive parallel data port
227	MD0	I/O	SDRAM Data bus terminal
228	VSSio	-	Connect to ground
229	MD1	I/O	SDRAM Data bus terminal
230	VSS	-	Connect to ground
231,232	MD2,3	I/O	SDRAM Data bus terminal
233	VDDio	-	Power supply terminal 3.3V
234~236	MD4~6	I/O	SDRAM Data bus terminal
237	VSSio	-	Connect to ground
238~240	MD7~9	I/O	SDRAM Data bus terminal

■ SST39VF160-7CEK (IC509) : 16M EEPROM

1. Pin layout



2. Block diagram

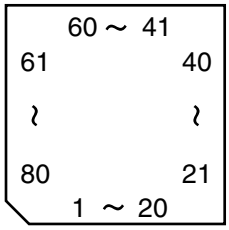


3. Pin function

Symbol	Pin name	Function
A19~A0	Address Inputs	To provide memory addresses. During sector erase A19~A11 address lines will select the sector. During block erase A19~A15 address lines will select the block.
DQ15~DQ0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when /OE or /CE is high.
/CE	Chip Enable	To activate the device when /CE is low.
/OE	Output Enable	To gate the data output buffers.
/WE	Write Enable	To control the write operations.
VDD	Power Supply	To provide 3-volt supply (2.7V-3.6V).
Vss	Ground	
NC	No Connection	

■ UPD780232GC-044(IC2):System controller

1.Pin layout



2.Pin function

Pin No.	Symbol	I/O	Description
1	VDD1	-	Power supply terminal (+)
2	VSS1	-	Connect to ground
3	X1	I	Main system clock oscillation terminal
4	X2	O	Main system clock oscillation terminal
5	IC(VPP)	-	Internal connection (connect to VSS1)
6	RESET	I	System reset input
7	SCK	I/O	Serial clock input/output of serial interface
8	RXD	I	Serial data input of serial interface
9	TXD	O	Serial data output of serial interface
10	POWERSW	I	Power switch (S1) input terminal
11	AVCO	O	AV Compulink output terminal
12	INTP	I/O	8 bit input/output port
13	P.ON	O	Power ON signal output
14	RESET	O	CPU Reset output
15	AVCI	I	AV Compulink input terminal
16	CS	I	Chip select input
17	REMO	I	Remote controller signal input
18	AVSS	-	Connect to ground for A/D converter
19	ANI3	I	Operation switch (S2,S3) input terminal
20	ANI2	I	Operation switch (S4~S7) input terminal
21	ANI1	-	Connect to ground
22	ANI0	-	Connect to ground
23	VSS0	-	Connect to ground for port section
24	AVDD	-	Standard voltage input for analog power supply of A/D converter
25	VDD0	-	Power supply terminal (+) for port section
26,27	STANDBYRED	O	Standby LED control signal output (red)
28,29	STANDBYGRN	O	Standby LED control signal output (green)
30,31	PRORED	O	Progressive LED control signal output (red)
32,33	PROGRN	O	Progressive LED control signal output (green)
34	AUDIOLED	O	DVD Audio LED control signal output
35		-	
36		-	Non connect
37	INT/PROG	O	Interlace/progressive switch signal output
38		O	Muting control signal output
39~58	S24~S5	O	FL Segment control signal output
59	VDD2	-	Power supply terminal (+) for driver section
60	VLOAD	-	Connected to pull down resistor for FL driver
61~64	S4~S1	O	FL Segment control signal output
65~67		-	Non connect
68~80	13G~1G	O	FL Grid control signal output

Glossary of term and abbreviations (for AV Decoder section)

3D	3-dimension
A/V	1)audio/video 2)audio/visual
ac	alternating current
ACLK	audio serial-data (bit) clock
AD	multiplexed address / data bus
ADC	analog-to-digital converter
AIN	digital audio input
ALE	address latch enable
ANSI/SMPTE	American National Standards Institute / Society of Motion Pictures and Television Engineers
AOP	Audio Output Processor
AXCLK	test-mode audio-PLL clock output
baud	unit of signaling speed equal to one code element per second
Cb	blue color difference component (in accordance with the CCIR 601 specifications)
CCIR	Consultative Committee on International Radio
CD	compact disc
CD-DA	compact disc-digital audio
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
Cr	red color difference component (in accordance with the CCIR 601 specifications)
CSS	Content Scrambling System
CTS	Clear To Send
CVBS	Composite Video Blank and Sync
DAC	Digital-to-Analog Converter
dc	direct current
DEMUX	DEMUX Engine
DSP	Digital Signal Processing
DTS	Digital Theater System
DVD	Digital Versatile Disc
EAV	End Active Video
EAV/SAV	End Active Video / Start Active Video
EEI	Enable Error Interrupt
EEPROM	Electrically Erasable Programmable Read-Only Memory
FS	FIFO Status
GPIO	General Purpose Input/Output
HDCD	High Definition Compatible Digital
HDTV	High-Definition television
HSYNC	Horizontal sync
I/O	Input/Output
IEC	International Electrotechnical Commission
IOM	Current (I) Output Minus (complementary shared current path to Video DAC current paths)
IR	infrared
ITU	International Telecommunications Union
LA	Latched Address Bus
LCLK	oscillator clock (derived from internal crystal oscillator)
Lfe	Low-frequency effect
LRCLK	Left/Right clock
LSB	Least Significant Bit
Mb	Megabit
MB	Megabyte

MCLK	primary or master clock
MHz	Megahertz
MIPS	Million Instructions Per Second
MmCPU	Mediamatics CPU (synonym for internal RISC CPU)
MP3	Moving Picture Experts Group Layer-3 Audio (audio file format / extension)
MPEG1 audio	A digital audio format mainly used in video CDs. It is based on the moving picture expert group (MPEG1) format, a data compression technology.
MPEG2 audio	A digital audio format mainly used in Europe and Australia. It provides high quality, multi-channel audio of up to eight channels in the same was as Dolby Digital and DTS. It is based on the MPEG2 format, a data compression technology more improved than MPEG1
NOP	No Operation
NTSC	1)National Television System Committee 2)Worldwide video standard in North America and Japan
NTSC-M	Version of NTSC used in certain parts of the world (Brazil)
OSD	On-screen display
PAL	Phase alteration by line
PCM	Pulse Code Modulation
PCMCLK	PCM audio-data over-sampling clock
PCS	1)Picture Control and Size 2)Perpheral Chip Select
PLL	Phase Lock Loop
PQFP	Plastic Quad Flat Pack (Package)
PWM	Pulse Width Modulator
r/w	Read/Write access
RAM	Random Access Memory
RGB	Red-Green-Blue (color model)
RISC	Reduced Instruction Set Computer
ROM	Read-Only Memory
RXD	Receive signal
RW	Readable / Write able
SAV	Start Active Video
SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televiseurs (connector used in Europe to connect many kinds of audiovisual equipment)
SCLK	Secondary or slave clock
SDRAM	Synchronous Dynamic Random Access Memory
S/PDIF	Sony / Philips Digital Interface
S/PDIFCLK	clock associated with the S/PDIF output
SRAM	Static Random Access Memory
SSP	Synchronous Serial Port
TXD	transmit signal
UART	Universal Asynchronous Receiver-transmitter
USART	Universal Synchronous / Asynchronous Receiver / Transmitter
VGA	Video Graphics Array
VIO	Video Input / Output
VREF	Voltage REFerence
Vref	Vertical reference
VSSA	quiet analog ground
VSYNC	Vertical sync
XBUS	External peripheral bus
XIO	External Input / Output
Y	Luminance component (in accordance with the CCIR 601 specifications)
YCbCr	Luminance component, blue color difference component, red color difference component (in accordance with the CCIR 601 specifications)

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